Panasonic®

PROGRAMMABLE CONTROLLER

FP2/FP2SH

User's Manual

ARCT1F320E-12

2012.9 | panasonic.net/id/pidsx/global

Safety Precautions

Observe the following notices to ensure personal safety or to prevent accidents.
To ensure that you use this product correctly, read this User's Manual thoroughly before use.
Make sure that you fully understand the product and information on safety.
This manual uses two safety flags to indicate different levels of danger.

WARNING

If critical situations that could lead to user's death or serious injury is assumed by mishandling of the product.

-Always take precautions to ensure the overall safety of your system, so that the whole system remains safe in the event of failure of this product or other external factor.
-Do not use this product in areas with inflammable gas. It could lead to an explosion.
-Exposing this product to excessive heat or open flames could cause damage to the lithium battery or other electronic parts.
-Battery may explode if mistreated. Do not recharge, disassemble or dispose of fire.

CAUTION

If critical situations that could lead to user's injury or only property damage is assumed by mishandling of the product.

-To prevent excessive exothermic heat or smoke generation, use this product at the values less than the maximum of the characteristics and performance that are assured in these specifications.
-Do not dismantle or remodel the product. It could cause excessive exothermic heat or smoke generation.
-Do not touch the terminal while turning on electricity. It could lead to an electric shock.
-Use the external devices to function the emergency stop and interlock circuit.
-Connect the wires or connectors securely.
The loose connection could cause excessive exothermic heat or smoke generation.
-Ground the protective earth (PE) terminal (Class D grounding). Failure to do so could lead to an electric shock.
-Do not allow foreign matters such as liquid, flammable materials, metals to go into the inside of the product. It could cause excessive exothermic heat or smoke generation.
-Do not undertake construction (such as connection and disconnection) while the power supply is on. It could lead to an electric shock.

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PLC_BATPE

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Before You Start

Operating environment
(Use the unit within the range of the general specifications when installing)

- **Ambient temperatures:0 to +55 °C**
- **Ambient humidity: 30% to 85% RH (at 25 °C, non–condensing)**
- **For use in pollution Degree 2 environment.**
- **Do not use it in the following environments.**
  - **Direct sunlight**
  - **Sudden temperature changes causing condensation.**
  - **Inflammable or corrosive gas.**
  - **Excessive airborne dust, metal particles or saline matter.**
  - **Benzine, paint thinner, alcohol or other organic solvents or strong alkaline solutions such as ammonia or caustic soda.**
  - **Direct vibration, shock or direct drop of water.**
  - **Influence from power transmission lines, high voltage equipment, power cables, power equipment, radio transmitters,or any other equipment that would generate high switching surges. (100mm or more)**

About static electricity

- **Do not touch connector pins directly to prevent static electricity from causing damage.**
- **Always rid yourself of any static electricity before handling this product.**

Wiring the Power Supply to the Control Unit

- **Use a power supply wire that is thicker than 2 mm^2 (AWG14), and twist it.**
- **The unit has sufficient noise immunity against the noise generated on the power line.**
  However, it is recommended to take measures for reducing noise such as using a isolating transformer before supplying the power.
- **Allocate an independent wiring for each power supplying line, input/output device and operating device.**
  If using a power supply without a protective circuit, power should be supplied through a protective element such as a fuse.
- **Use the same power supply system for the CPU backplane and expansion backplane so that they are turned on and off simultaneously.**

Power supply sequence

- **In order to protect the power supply sequence, make sure to turn off the PLC before the input/output power supply. If the input/output power supply is turned off before the PLC, or if the PLC is not shut off momentarily, the controller detects change of input level, and might conduct an unexpected operation.**

Before Turning On the Power (☛ Chapter 4 and Chapter 5)

When turning on the power for the first time, be sure to take the precautions given below.

- **When performing installation, check to make sure that there are no scraps of wiring, particularly conductive fragments, adhering to the unit.**
- **Verify that the power supply wiring, I/O wiring, and power supply voltage are all correct.**
- **Sufficiently tighten the installation screws and terminal screws.**
- **Set the mode selector to PROG. mode.**

Before Entering a Program (☛ Chapter 5)

Be sure to perform a program clear operation before entering a program.

When using FPWIN GR software

Procedure:

1. **Execute “FPWIN GR”.**
2. **ON the “Online” menu, select “Online Edit Mode”.**
3. **ON the “Edit” menu, select “Clear Program”.**

Battery

Do not install the battery when it is not used.

There is a possibility of leak if the battery remains discharged.

Special Precautions

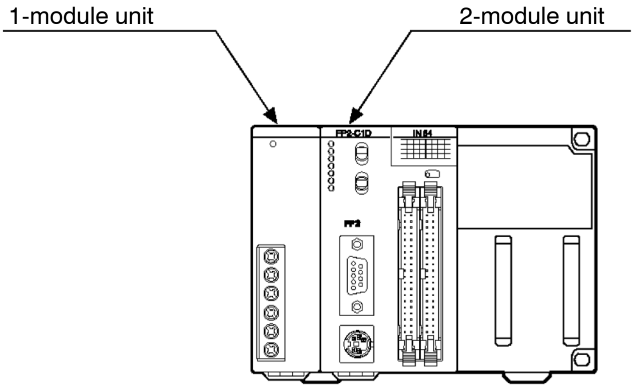
With the FP2

The FP2 uses the term “module” when express the size of the unit or backplane.

The unit installation sizes come in two sizes: the basic 1-module size, and the 2-module size that is twice as wide.

The 1-module unit is the size that physically takes up the space of one guide on the backplane.

The 2-module unit is the size that physically takes up the space of two guides on the backplane.



Backplane Selection

Following two kinds of backplanes are available.
1) FP2 backplane (AFP25***) (Color of letters on the printed board: White)
2) FP2 backplane H type (AFP25****H) (Color of letters on the printed board: Yellow)
These two backplanes cannot be used in combination.
Carefully select the type of backplanes before you order.

The selection of the backplane should be based on the total number of modules to be used in the system. In other words, the module number of the backplane must be greater than or equal to the total number of modules for the system. So be sure to select a backplane that allows the installation of all the required units.

When using the FP3, FP10SH, or Other Units

Backplane slot number

The backplane for the FP2 is specified by the total number of slots, i.e., 14-module type, including the connectors for the power supply unit and CPU. The number of connectors (or slots) remaining for the I/O units and intelligent units is then the module number of the backplane minus the number of modules for the power supply unit and CPU. Similarly, the number of connectors (or slots) remaining for the I/O units on expansion backplanes is the module number of the backplane minus the number of modules for the power supply unit.

Expansion backplanes

1. FP2 backplane

- Does not support expansion with 5-module type backplanes.
- Backplanes that are not the 5-module type can be used as expansion backplanes.

2. FP2 backplane H type

- This backplane is functionally equivalent to the backplane for FP3.
- There are the basic backplane H type for installing I/O units and the expansion backplane H type for adding I/O units more.
- The basic backplane cannot be used as an expansion backplane.

Removal and Installation of Expansion Memory Unit

During removal and installation of expansion memory unit, the contents of the internal RAM may be erased, so be sure to save a copy of the program and data onto a disk before beginning the operations.

Use programming tool software (NPST−GR/FPWIN GR) for backup purposes.

Before rewriting the backed up program and data to the programmable controller, be sure to clear the program in the programmable controller.

With the FP2SH

Programming Tool Restrictions

The following tool software is required in order to program the FP2SH.
“FPWIN GR”
“NPST−GR” Ver. 4.6 or a subsequent version

Request Concerning Program Storage

To prevent the accidental loss of programs, the user should consider the following measures.

Drafting of documents

To avoid accidentally losing programs, destroying files, or overwriting the contents of a file, documents should be printed out and then saved. Disks should be organized to assure safe maintenance.

Specifying the password carefully

The password setting is designed to avoid programs being accidentally overwritten. If the password is forgotten, however, it will be impossible to overwrite the program even if you want to. Also, if a password is forcibly bypassed, the program is deleted. When specifying the password, note it in the specifications manual or in another safe location in case it is forgotten at some point.

Saving programs to the ROM

In order to prevent programs from being lost if the backup battery runs down, and to prevent accidental overwriting of programs in the workplace, we recommend saving programs entered in the RAM to the ROM. If the PLC is used over a long period of time, this concern applies particularly to programs that are built into the device when shipped.

Check the manuals for specifications and other items pertaining to usage.

FP series Programming Manual

Compatibility with CPU unit, and Precautions

Comparison of Specifications

Items			FP2 CPU	FP2SH CPU	FP10SH CPU	
			FP2−C1, FP2−C1D, FP2−C1A,FP2−C1SL	FP2−C2L, FP2−C2, FP2−C2P,FP2−C3P	AFP 6221V3	AFP 6211V3
Controllable I/O points		Basic construction	Using Backplanes: Max. 768 points (12 modules) Using Backplanes H type: Max. 512 points (8 modules)		Max. 512 points	
		Expanded construction	Using Backplanes: Max. 1,600 points (25 modules) Using Backplanes H type: Max. 2,048 points (32 modules)		Max. 2,048 points	
		Using remote I/O system	Max. 2,048 points	Max. 8,192 points	Max. 8,192 points	
Program capacity		Internal memory	Approx. 16k steps	Approx. 60k steps (For FP2−C3P, approx. 120k steps)	Approx. 30k steps	
		Using expansion memory	Approx. 32k steps	—	Approx. 60k steps/ 120k steps	
Operation speed (typical value)		Basic instructions	From 0.35μs per instruction	From 0.03μs per instruction	From 0.04μs per instruction	From 0.10μs per instruction
		High-level instructions	From 0.93μs per instruction	From 0.06μs per instruction	From 0.08μs per instruction	From 0.20μs per instruction
Operation memory points	Relays	External input (X)	2,048 points	8,192 points	8,192 points	
		External output (Y)	2,048 points	8,192 points	8,192 points	
		Internal relays (R)	4,048 points	14,192 points	14,192 points	
		Timer/counter (T/C)	Total 1,024 points	Total 3,072 points	Total 3,072 points	
		Link relays (L)	2,048 points	10,240 points	10,240 points	
		Pulse relays (P)	1,024 points	2,048 points	2,048 points	
		Alarm relays (E)	None	2,048 points	2,048 points	
	Memory areas	Data registers (DT)	6,000 words	10,240 words	10,240 words	
		File registers (FL)	0 to 14,333 words (when expanding: 0 to 30,717 words)	FP2−C2L: 32,765 words FP2−C2, FP2−C2P, FP2−C3P: 32,765 words × 3 banks	32,765 words	
		Link data registers (LD)	256 words	8,448 words	8,448 words	
		Timer/counter set value area (SV)	1,024 words	3,072 words	3,072 words	
		Timer/counter elapsed value area (EV))	1,024 words	3,072 words	3,072 words	
		Index registers (I0 to ID)	14 words	14 words × 16 banks	14 words × 16 banks	
Comment input function			Optional function	Built−in (Internal) function	Optional function	
Clock/calendar function			Optional function	Built−in (Internal) function	Built−in (Internal) function	
ROM operation function			Optional function	FP2−C2L, FP2−C2: Optional function FP2−C2P, FP2−C3P: Built−in (Internal) function	Optional function	

Compatibility of FP2SH and FP2, and Precautions

Hardware Compatibility

Most of the units and related products used with the FP2SH can be used with the FP2, but the following differences should be noted.

Some optional memory units cannot be used.

The only memory unit that can be used with the FP2SH CPU FP2−C2 or FP2−C2L” is the ”Part number FP2−EM7 or Model number AFP2208”.
The FP2 memory units “Part numbers FP2−EM1, FP2−EM2, FP2−EM3, and FP2−EM6” cannot be used.

The types of optional ROMs are different.

The only ROM that can be used with the FP2SH CPU unit ”FP2−C2” is the ”Model number AFP5208 or AFP5209”. The nonvolatile memory implemented memory unit ”Model number AFP2208” can be also used.
The FP2 ROM “Part number AFP2204” and “Part number AFP2205” cannot be used.

The backup battery types are different.

The backup battery for the FP2SH CPU is the “Part number AFP8801” battery with a connector.
The “Part number AFC8801” battery for the FP2 CPU cannot be used.

The calendar timer and comment memories have been installed in advance.

These have already been installed in the FP2SH CPU, and no optional units are needed.

ROM operation functions in the FP2SH

CPUs that support IC memory cards (FP2−C2P and FP2−C3P) have an internal FROM used as a program memory. The internal FROM cannot be replaced.

Software Compatibility

The FP2SH has a higher level of compatibility than the FP2, so there are no functions that cannot be used with the FP2SH. Other factors, such as the number of device points, should be confirmed by checking the specifications comparison table on the previous page.

IC memory cards for the FP2SH

The existing model number becomes the one to be discontinued because of the termination of manufacturing IC memory cards by the parts manufacturer. When placing a new order, specify the new product number.

Termination of Production

Type	Memory capacity	Model No.	Battery type
SRAM	2MB	AIC52000	Internal secondary battery (Rechargeable type)

New product

Type	Memory capacity	Model No.	Battery type
SRAM	2MB	AFP2209	Lithium Battery (Interchangeable type)

☞ Notes

For AFP2209

- **An interchangeable lithium battery is used. When you use for the first time, install the battery included.**

For AIC52000

- **Memory backup of the SRAM type of IC memory card (AIC52000) Is handled by an internal secondary battery. When the battery is used for the first time, power must be supplied for at least 24 hours to charge it fully. When the battery is fully charged, data is backed up for more than three months with out the power being turned on. Normally, the card should be installed in the PLC and power supplied when using it. Failing to charge the battery periodically can reduce the backup period and the service life of the battery. The backup battery cannot be replaced.**

Compatibility of FP2/FP2SH and FP10SH, and Precautions

Hardware Compatibility

The unit, backplane, and other components are not compatible.

The components for the FP2 are used with the FP2SH.

When using the FP2 backplane (AFP25), the maximum number of expansion points is lower.**

With the FP10SH and FP2 backplane H type (AFP25**H), up to three expansion boards can be used, and a maximum of 2048 points controlled, but if using the FP2 backplane with the FP2/FP2SH, only one expansion board can be used, and a maximum of 1600 points controlled.

Different types of IC memory cards are used.

The only type of IC card that can be used with the "Part number FP2−C2P and FP2−C3P" FP2SH CPU is the IC memory card (small PC card). The IC memory card for the FP10SH cannot be used.

Software Compatibility

With the FP2SH, in comparison with the FP10SH, there are no functions that cannot be used. For other detailed specifications, check the specifications comparison table on the previous page.

Programming Tool Restrictions

Restrictions on usable programming tools depending on the units

Type of programming tool		Type of unit	
		FP2	FP2SH
Windows software	FPWIN GR Ver.2	Used Note 1)	Used Note 1)
	FPWIN GR Ver.1	Used Note 1)	Used Note 1)
Windows software Conforms to IEC61131−3	FPWIN Pro Ver.6	Used	Used Note 2)
	FPWIN Pro Ver.5	Used Note 3)	Used Note 3)
Handy programming unit	AFP1113V2 AFP1114V2	Not used	Not used
	AFP1113 AFP1114	Not used	Not used
	AFP1111A AFP1112A AFP1111 AFP1112	Not used	Not used
FP Memory Loader	AFP8670 AFP8671	Used	Used Note 4)

Note 1) FPWIN GR Ver.2.91 or later version is necessary to use the FP2SH CPU (32k type).
FPWIN GR Ver.2.40 or later version is necessary to use the multi communication unit.
FPWIN GR Ver.2.71 or later version is necessary to use the MEWNET−VE Link Unit.
The FNS Unit and FMU Unit cannot use to FPWIN GR.

Note 2) FPWIN Pro Ver.6.3 or later version is necessary to use the FP2SH CPU (32k type).

Note 3) FPWIN Pro Ver.5.02 or later version is necessary to use the multi communication unit.
−FPWIN Pro Ver.5.24 or later version is necessary to use the MEWNET−VE Link Unit.
−FPWIN Pro Ver.5.24 or later version is necessary to use the FNS Unit.
−FPWIN Pro Ver.5.3 or later version is necessary to use the FMU Unit.

Note 4) FP Memory Loader Ver.2.1 or later version is necessary to use the FP2SH CPU (32k type). When using FP2SH CPU (120k type), only the 1st program and comments can be transferred.

Note: Precautions concerning version upgrade

- **In case of using FPWIN GR Ver.1, please purchase upgrade model FPWIN GR Ver.2.**
- **FPWIN GR Ver. 2.0 can be upgraded to Ver. 2.1 or later free of charge at our web site.**
- **FPWIN Pro Ver. 6.0 can be upgraded to Ver. 6.1 or later free of charge at our web site (http://industrial.panasonic.com/ac/e/dl_center/software/).**

Chapter 1

Overview

1.1 System Configuration

1.1.1 Basic Configuration by Number of Slots

The building block scheme allows you to combine units as desired.

Five types of backplanes and Two types of backplanes H types are available for the FP2/FP2SH. A variety of input/output units can be installed as desired on the back-plane.

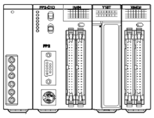
Although most of the I/O units and intelligent units can be combined freely in the layout, you should check the following three points when selecting your units:

– Restrictions on unit types ☛ section 1.2.2.1

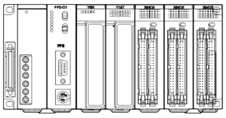
– Limitations on the internal current consumption ☛ section 1.2.2.2

– Limitations on the number of modules of the backplane ☛ page 1 – 4

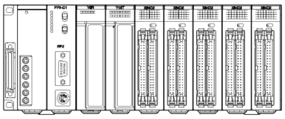
FP2 backplane



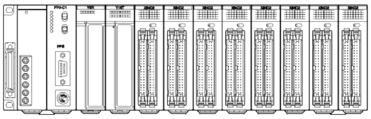
5 modules



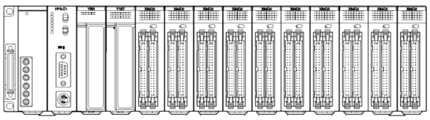
7 modules



9 modules

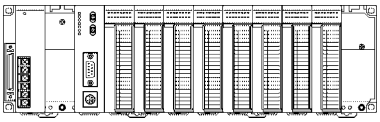


12 modules

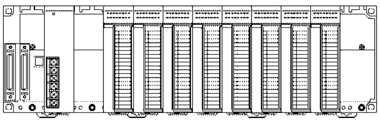


14 modules

FP2 backplane H type



Basic backplane (11 modules)



Expansion backplane (10 modules)

Following two kinds of backplanes are available.
1) FP2 backplane (AFP25***)
2) FP2 backplane H type (AFP25****H)
These two backplanes cannot be used in combination.
Carefully select the type of backplanes before you order.

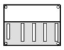
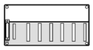
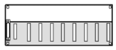
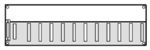
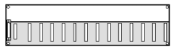
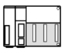
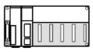
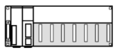
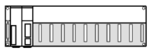
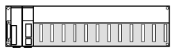
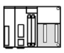
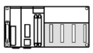
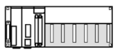
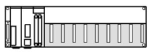
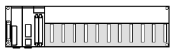
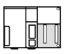
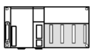
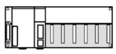
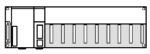
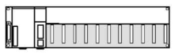
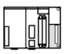
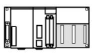
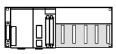
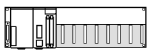
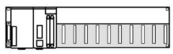
Restriction on the number of modules of the backplane (For master backplane)

The number of units that can be installed is determined by the number of modules of the backplane used, the power supply unit to be installed, and the CPU.

1 module type CPU	Standard type CPU
2 modules type CPU	CPU with 64-point input, CPU with S-LINK
1 module type power supply unit	100V 2.5A, 200V 2.5A
2 modules type power supply unit	100 to 240V 5A, 24V DC 5A

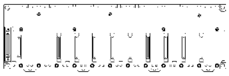
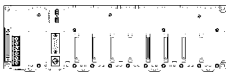
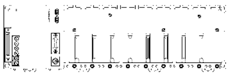
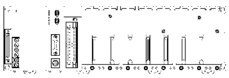
CPU backplane

FP2 backplane

	5-module type	7-module type	9-module type	12-module type	14-module type
					
1 module type CPU and 1 module type power supply unit	3 slots free 	5 slots free 	7 slots free 	10 slots free 	12 slots free 
2 modules type CPU and 1 module type power supply unit	2 slots free 	4 slots free 	6 slots free 	9 slots free 	11 slots free 
1 module type CPU and 2 module type power supply unit	2 slots free 	4 slots free 	6 slots free 	9 slots free 	11 slots free 
2 modules type CPU and 2 module type power supply unit	1 slot free 	3 slots free 	5 slots free 	8 slots free 	10 slots free 

* slots free: Number of slots where units can be installed

FP2 backplane H type

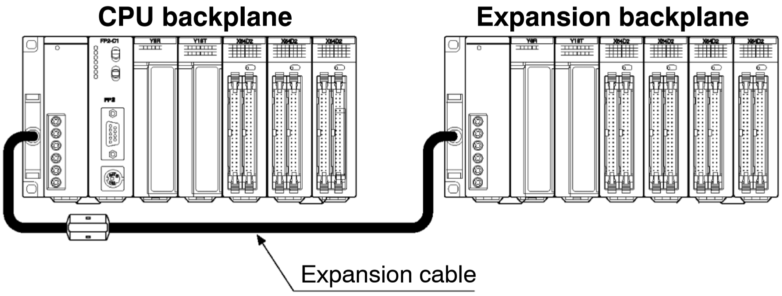
	11−module type 
1 module type CPU and 1 module type power supply unit	8 slots free 
2 module type CPU and 1 module type power supply unit	7 slots free 
1 module type CPU and 2 module type power supply unit	8 slots free 
2 module type CPU and 2 module type power supply unit	7 slots free 

A maximum of eight I/O units (including the unit built in the CPU) can be controlled per backplane. Even if further I/O units are installed, they are not recognized.

Note) When using the CPU unit with S−LINK, seven slots are free, however, the units actually usable are only six. (Refer to Chapter 3 I/O Allocation.)

1.1.2 Expansion of Backplane

FP2 backplane



Only one backplane can be added-on for expansion.
Expansion is simply connecting a new backplane with a special expansion cable. Any backplane other than a 5-module type can be used for expansion.

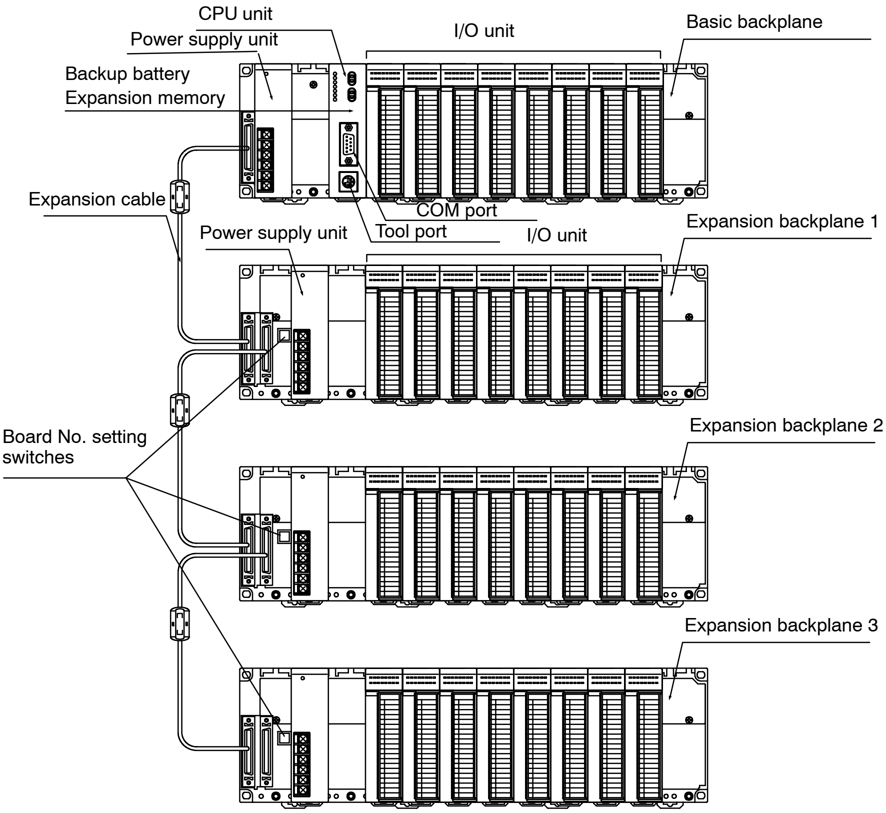
☞ Notes

- **A 5-module type backplane cannot be expanded.**
- **A 5-module type backplane cannot be added on for expansion.**
- **Only one backplane can be added-on for expansion.**
- **A power supply unit is also necessary on an expansion back-plane.**

☛ next page

- **Do not install a CPU on an expansion backplane.**
- **There is no need to make the number of modules on the expansion backplane equal to the number of modules on the CPU backplane.**

FP2 backplane H type



The basic FP2 backplane H type that the CPU unit can be installed and the expansion backplane H type that only the I/O units and the intelligent I/O units can be installed are available.
A maximum of eight I/O units (including the unit built in the CPU) can be controlled per backplane. Even if further I/O units are installed, they are not recognized.

Up to three expansion backplanes can be added on for expansion.

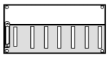
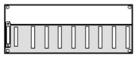
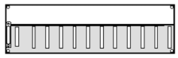
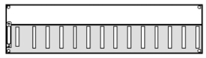
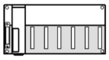
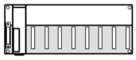
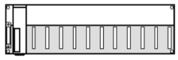
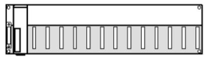
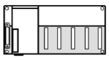
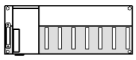
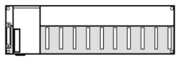
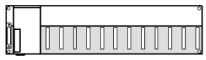
Use the board No. setting switches on the board to distinguish the expansion backplane.

A power supply unit is also necessary on an expansion backplane.

Restriction on the number of modules of the backplane (For expansion backplane)

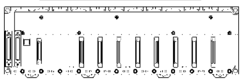
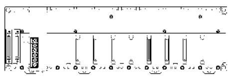
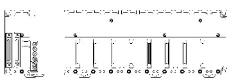
The number of units that can be installed is determined by the number of modules of the backplane used and the power supply unit to be installed.

FP2 backplane

	7-module type 	9-module type 	12-module type 	14-module type 
1 module type power supply unit	6 slots free 	8 slots free 	11 slots free 	13 slots free 
2 module type power supply unit	5 slots free 	7 slots free 	10 slots free 	12 slots free 

* slots free: Number of slots where units can be installed

FP2 backplane H type

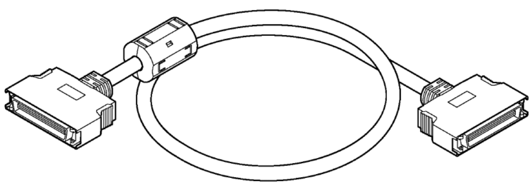
	10-module type 
1 module type power supply unit	8 slots free 
2 module type power supply unit	8 slots free 

Note) Although the connectors for installing I/O units are free with a 1–module type power supply unit, they cannot be used.

Expansion cable

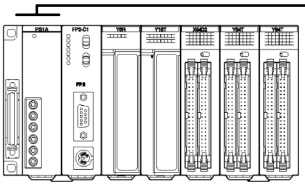
Order number	Length	Ferrite core
FP2–EC	60 cm	1
FP2–EC2	2 m	2

Note) With the backplalne H type, the total cable length can be arranged within 3.2 m.

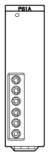


1.2 Unit Types and Combinations

1.2.1 Line-Up of Backplanes and Units

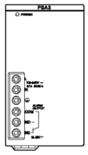


Power supply units



100V AC 2.5A type
(FP2−PSA1)

200V AC 2.5A type
(FP2−PSA2)



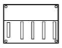
100 to 240V AC 5A type
(FP2−PSA3)

24V DC 5A type
(FP2−PSD2)

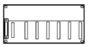
Backplanes

(for CPU and expansion backplanes)

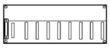
The 5−module type backplane can not be used for expansion.



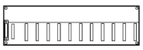
5-module type
(FP2−BP05)



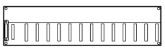
7-module type
(FP2−BP07)



9-module type
(FP2−BP09)

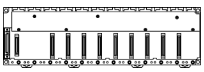


12-module type
(FP2−BP12)

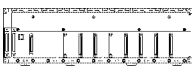


14-module type
(FP2−BP14)

Backplanes H type

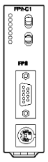


11-module type (Basic)
FP2−BP11MH (AFP25011MH)

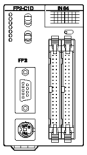


10-module type (Expansion)
FP2−BP10EH (AFP25010EH)

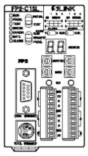
FP2 CPU



Standard type CPU
(FP2−C1)

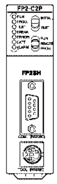


CPU with 64-point input
(FP2−C1D)

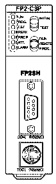


CPU with S-LINK
(FP2−C1SL)

FP2SH CPU

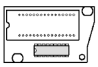


Standard type:
32k step: FP2−C2L (AFP2221)
60k step: FP2−C2 (AFP2231)

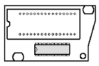


Small PC card compliant type:
60k step: FP2−C2P (AFP2235)
120k step: FP2−C3P (AFP2255)

Optional memories For FP2



FP2−EM1
FP2−EM2



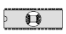
FP2−EM3
FP2−EM6
FP2−EM7

Type of memory unit

Part No.	Comment input function	Clock/ calendar function	With 16k expansion RAM	ROM socket
FP2−EM1	A	A	N/A	N/A
FP2−EM2	A	A	A	N/A
FP2−EM3	A	A	A	A
FP2−EM6	N/A	N/A	A	A
FP2−EM7	N/A	N/A	N/A	A

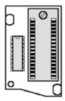
A: Available, N/A: Not available

FROM **FP2−EM4**

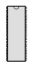


EPROM **FP2−EM5**

Memory unit for FP2SH



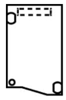
Memory unit ROM socket
(FP2−EM7)



F−ROM
(AFP5208)

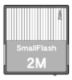
EP−ROM
(AFP5209)

Memory unit for FP2SH



Memory unit F−ROM implemented)
(AFP2208)

Small PC card for FP2SH



FROM type IC memory card
(AIC50020)

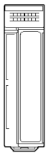
SRAM type IC memory card
(AIC52000)
Discontinued products

SRAM type IC memory card
(AFP2209)

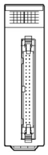
Option

Product name		Product number
Dummy unit		AFP2300
Battery	**Lithium battery (button)**	AFC8801
	Lithium battery	AFP8801
Battery for AFP2209		AFP2806
Terminal block for FP2 I/O unit		AFP2800
Set of connector for wire−pressed terminal cable (2 pieces)		AFP2801
Set of flat cable connector (2 pieces)		AFP2802

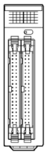
Input, Output and I/O mixed units



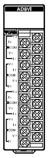
16-point DC input **(FP2−X16D2)**
16-point transistor output NPN type **(FP2−Y16T)**
16-point transistor output PNP type **(FP2−Y16P)**
6-point relay output type **(FP2−Y6R)**
16-point relay output type **(FP2−Y16R)**



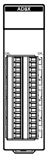
32-point DC input **(FP2−X32D2)**
32-point transistor output NPN type **(FP2−Y32T)**
32-point transistor output PNP type **(FP2−Y32P)**



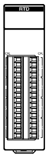
64-point DC input **(FP2−X64D2)**
64-point transistor output NPN type **(FP2−Y64T)**
64-point transistor output PNP type **(FP2−Y64P)**
32-point input/ 32-point output NPN type **(FP2−XY64D2T)**
32-point input/output (NPN) with on pulse catch input **(FP2−XY64D7T)**
32-point input/ 32-point output PNP type **(FP2−XY64D2P)**
32-point input/output (PNP) with on pulse catch input **(FP2−XY64D7P)**



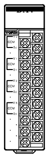
Analog input
FP2−AD8VI



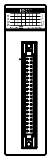
Analog output
FP2−AD8X



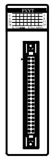
RTD input
FP2−RTD



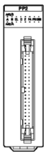
Analog output
FP2−DA4



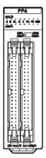
High speed counter
FP2−HSCT(NPN)
FP2−HSCP(PNP)



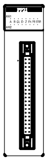
Pulse I/O
FP2−PXYT(NPN)
FP2−PXYP(PNP)



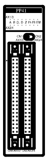
Positioning
(2−axis)
FP2−PP2



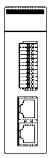
Positioning
(4−axis)
FP2−PP4



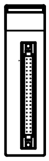
Positioning (2−axis)
Multifunction
Transistor **FP2−PP21**
Line driver **FP2−PP22**



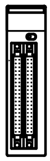
Positioning (4−axis)
Multifunction
Transistor **FP2−PP41**
Line driver **FP2−PP42**



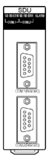
Positioning RTEX
FP2−PN2AN
(2−axis)
FP2−PN4AN
(4−axis)
FP2−PN8AN
(8−axis)



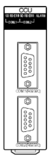
Positioning (2−axis)
(Interpolation)
Transistor **FP2−PP2T**
Line driver
FP2−PP2L



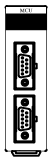
Positioning (4−axis)
(Interpolation)
Transistor **FP2−PP4T**
Line driver **FP2−PP4L**



Serial data
FP2−SDU

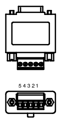


C.C.U
FP2−CCU



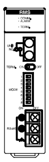
MCU
FP2−MCU

Communication Block
FP2−CB232
FP2−CB422

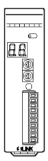


Communication Block
FP2−CB485

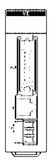
Multi−wire link
FP2−MW



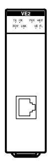
Remote I/O Slave
FP2−RMS



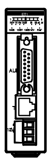
S-LINK
FP2−SL2



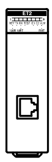
MEWNET−VE link
FP2−VE



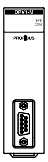
MEWNET−VE2 link
FP2−VE2



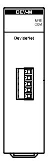
ET−LAN
FP2−ET1



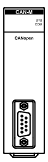
ET−LAN2
FP2−ET2



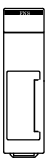
FMU
FP2−DPV1−M



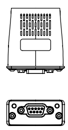
FMU
FP2−DEV−M



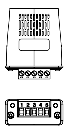
FMU
FP2−CAN−M



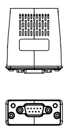
FNS
FP2−FNS



Communication Block
PROFIBUS
(AFPN−AB6200)



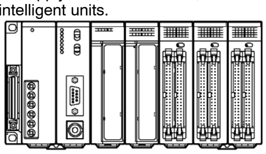
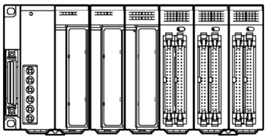
Communication Block
DeviceNet
(AFPN−AB6201)



Communication Block
CANopen
(AFPN−AB6218)

1.2.2 Combinations That Can be Used and Restrictions

1.2.2.1 Restrictions on Unit Types

System configuration \ Backplanes and units used	Backplane		Backplane H type		Power supply unit	CPU unit	Re-mote I/O slave unit	Input unit	Output unit	I/O mixed unit
	(5-module type)	(7-, 9-, 12-, 14-module type)	Basic (11–module type)	Expan-sion (10–module type)						
CPU backplane Install in order from the left to the right, the power supply unit, the CPU unit, the I/O and the intelligent units. 	A	A	A	N/A	A	A	N/A	A	A	A
Expansion backplane Install in order from the left to the right, the power supply unit, the I/O and the intelligent units. 	N/A	A	N/A	A *4	A	N/A	N/A	A	A	A
Slave station system backplane – **Master backplane for slave station system** Install in order from the left to the right, the power supply unit, the Remote I/O slave unit,the I/O and the intelligent units.*Replace the CPU on the CPU backplane with a remote I/O slave unit.	A	A	A	N/A	A	N/A	A	A	A	A
Slave station system backplane – **Expansion backplane for slave station system** Install in order from the left to the right, the power supply unit, the I/O and the intelligent units.* Same as the installa-tion of the expansion backplane.	A	A	A	A	A	N/A	N/A	A	A	A

Limitations on Combining Link Units

<table>
<tr><th>Unit type and mode</th><th>When CPU unit is FP2</th><th>When CPU unit is FP2SH</th></tr>
<tr><td>Computer communication unit</td><td>Only one unit (see note)</td><td rowspan="2">Can be installed within 5 units in combination with W link, CCU and MCU (PC link mode).</td></tr>
<tr><td rowspan="2">Multi–wire Link unit (MEWNET–W mode)</td><td>Can be installed within 3 units in combination with W link, CCU and MCU (PC link mode).</td></tr>
<tr><td colspan="2">Can be installed within 2 units in combination with MCU in PC (PLC) link mode.</td></tr>
<tr><td>Multi–wire Link unit (MEWNET–W2 mode)
ET–LAN unit</td><td>Up to 3 units can be used.
Up to 2 units out of 3, when including PC (PLC) link.</td><td>Up to 8 units can be used.
Up to 2 units out of 8, when including PC (PLC) link.</td></tr>
<tr><td rowspan="2">Multi Communication unit (PC (PLC) link mode)</td><td>Can be installed within 3 units in combination with W link, CCU and MCU.</td><td>Can be installed within 5 units in combination with W link, CCU and MCU.</td></tr>
<tr><td colspan="2">Can be installed within 2 units in combination with W link unit in PC (PLC) link mode.</td></tr>
<tr><td>Multi Communication unit (Computer link mode)</td><td colspan="2">Up to 8 units can be used.</td></tr>
<tr><td>MEWNET–VE Link Unit</td><td>Not Available</td><td>Can be installed within 2 units in combination with Multi Communication Unit.</td></tr>
</table>

Note

Depending on the location of the connected ports and the commands used for communication, up to 3 units can be used. For more details, refer to the Computer Communication Unit Manual.

Output unit	I/O mixed unit	Analog input unit	Analog output unit	High-speed counter unit	Pulse I/O unit	Positioning unit (PP2/PP4)	Positioning unit (Multi-function type)	Positioning unit RTEX	Positioning unit Interpolation type	Serial data unit	Computer communication unit	S-LINK unit	Multi-wire link unit			ET-LAN unit	Multi communication	MEW-NET-VE Link Unit	FNS unit	FMU unit
													MEW-NET-F mode	MEW-NET-W mode	MEW-NET-W2 mode					
A	A	A	A	A *1	A *1	A	A	A	A	A	A *2	A	A *3	A *2	A *2	A *2	A *2	A *2	A	A
A	A	A	A	A *1 *5	A *1 *5	A	A	A	A	A	N//A	A	A *3	N/A	N/A	N/A	A *2	N/A	A	A
A	A	N/A	N/A	A *6	A *6	A *7	N/A	N/A	N/A	A	N//A	A *8	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
A	A	N/A	N/A	A *6	A *6	A *7	N/A	N/A	N/A	A	N//A	A *8	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

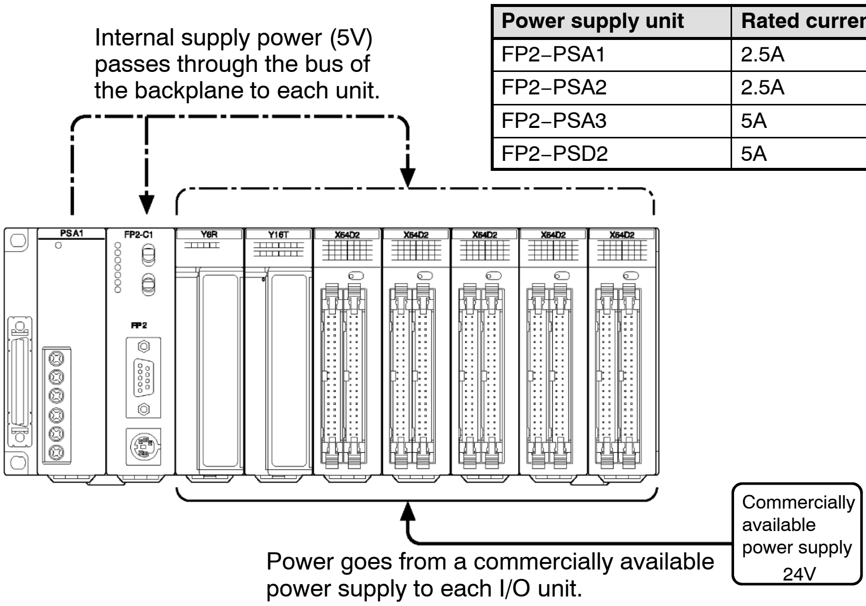
A: Available N/A: Not available

Notes

1) **When “Mode B: Unit with interrupt function” has been specified, the unit will be treated as interrupt unit, and 8 interrupts per unit will be available for use. However, when “Mode B” has been set for the unit, 2 units can be used with 1 CPU unit. When “Mode C: Intelligent unit that generate interrupts” has been specified, and 1 interrupt per unit will be available for use. However, when “Mode C” has been set for the unit, 8 units can be used with 1 CPU unit.**
2) **Check the limitations on combining link units given below.**
3) **In the MEWNET−F mode, up to four units can be used counting the CPU and expansion sides.**
4) **With the backplane H type, the total expansion cable length can be arranged within 3.2 m.**
5) **The unit cannot be installed on the 31st slot (last slot) when using the H−type backplane.**
6) **The interrupt function is not available for the backplane on the slave station system.**
7) **With the backplane on the slave station system, the time taken from the startup until the completion of positioning should be longer than a scan time.**
8) **With the backplane on the slave station system, I/O points cannot be set including 96 input points and 96 output points.**

1.2.2.2 Limitations on Current Consumption

Power supply unit	Rated current (at 5V)
FP2−PSA1	2.5A
FP2−PSA2	2.5A
FP2−PSA3	5A
FP2−PSD2	5A



Internal supply power (5V DC)

The 5V DC power used for driving the internal circuit of each unit is supplied from the power supply unit through the internal bus of the backplane.

External supply power (24V DC)

The 24V DC power supply used as the input power supply of the input units and the output circuit driving power of the output units are supplied from the external terminal of each unit.

For 24V power supply, commercially available power supply equipment is used.

Combining units and selecting a backplane

The current consumed by each unit is shown in the following pages.
Give consideration to the combination of units so that the rated capacity of 5V DC and 24V DC power supplies should not exceeded.

Example of current consumption calculation

The table below shows the combination of typical units on a 9-module type backplane.

Type	Number of units and backplane used	Current consumption at 5V DC (mA)	Current consumption at 24V DC (mA)
CPU (FP2−C1)	**1**	410	0
Backplane (FP2−BP09)	**1**	60	0
Input unit (FP2−X16D2)	**3**	60×3=180	8×16×3 = 384
Output unit (FP2−Y16R)	**4**	120×4=480	160×4=640
Total current consumption		1130	1024

Table of current consumption at 5V DC

Type				Part number	Current consumption at 5V DC (mA)
FP2 CPU				FP2–C1	410 or less
				FP2–C1D	530 or less
				FP2–C1SL	630 or less
				FP2–C1A	1060 or less
FP2SH CPU				FP2–C2L	750 or less
				FP2–C2	750 or less
				FP2–C2P	750 or less
				FP2–C3P	750 or less
Backplane				FP2–BP05	5 or less
				FP2–BP07	60 or less
				FP2–BP09	60 or less
				FP2–BP12	60 or less
				FP2–BP14	60 or less
Backplane H type				FP2–BP11MH	5 or less
				FP2–BP10EH	60 or less
Input unit	**DC input**	**16-point terminal type, 12 to 24V DC**		FP2–X16D2	60 or less
		32-point connector type, 24V DC		FP2–X32D2	80 or less
		64-point connector type, 24V DC		FP2–X64D2	100 or less
Output unit	**Relay output**	**6-point terminal type**		FP2–Y6R	50 or less
		16-point terminal type		FP2–Y16R	120 or less
	Transistor output	**16-point terminal NPN type**		FP2–Y16T	100 or less
		32-point connector NPN type		FP2–Y32T	130 or less
		64-point connector NPN type		FP2–Y64T	210 or less
		16-point terminal PNP type		FP2–Y16P	80 or less
		32-point connector PNP type		FP2–Y32P	130 or less
		64-point connector PNP type		FP2–Y64P	210 or less
I/O mixed unit	**32-point 24V DC input/32-point connector NPN output type**			FP2–XY64D2T, FP2–XY64D7T	160 or less
	32-point 24V DC input/32-point connector PNP output type			FP2–XY64D2P, FP2–XY64D7P	160 or less
Intelligent unit	**Analog input unit (Voltage/current type)**			FP2–AD8VI	400 or less
	Analog input unit (Channel type)			FP2–AD8X	300 or less
	RTD input unit			FP2–RTD	300 or less
	Analog output unit			FP2–DA4	600 or less
	High–speed counter unit	**NPN**		FP2–HSCT	450 or less
		PNP		FP2–HSCP	450 or less
	Pulse I/O unit	**NPN**		FP2–PXYT	500 or less
		PNP		FP2–PXYP	500 or less
	Positioning unit	**2-axis type**		FP2–PP2	225 or less
		4-axis type		FP2–PP4	400 or less
	Positioning unit (Multi-function type)	**2-axis type**	**Transistor output type**	FP2–PP21	200 or less
			Line driver output type	FP2–PP22	200 or less
		4-axis type	**Transistor output type**	FP2–PP41	350 or less
			Line driver output type	FP2–PP42	350 or less
	Positioning unit RTEX	**2-axis type**		FP2–PN2AN	300 or less
		4-axis type		FP2–PN4AN	300 or less
		8-axis type		FP2–PN8AN	300 or less
	Positioning unit (Interpolation type)	**2-axis type**	**Transistor output type**	FP2–PP2T	300 or less
			Line driver output type	FP2–PP2L	300 or less
		4-axis type	**Transistor output type**	FP2–PP4T	300 or less
			Line driver output type	FP2–PP4L	300 or less
	Serial data unit			FP2–SDU	60 or less
	Multi communication unit with Communication block (1–unit or 2–unit)			FP2–MCU	480 or less

☛ next page

Type				Part number	Current consumption at 5V DC (mA)
Intelligent unit	C.C.U.			FP2–CCU	60 or less
	S-LINK unit			FP2–SL2	130 or less
	Multi-wire link unit			FP2–MW	220 or less
	Remote I/O Slave Unit			FP2–RMS	150 or less
	ET–LAN unit			FP2–ET1	670 or less
	MEWNET–VE Link unit			FP2–VE	670 or less
	FNS unit	FNS unit		FP2–FNS	55 or less
		FP–FNS Block	PROFIBUS	AFPN–AB6200	230 or less
			Device Net	AFPN–AB6201	65 or less
			CAN open	AFPN–AB6218	65 or less
	FMU unit	PROFIBUS		FP2–DPV1–M	450 or less
		Device Net		FP2–DEV–M	150 or less
		CAN open		FP2–CAN–M	450 or less

Table of current consumption at 24V DC

Type			Part number	Current consumption at 24V DC (mA)
Input unit	DC input	16-point terminal type, 12 to 24V DC	FP2–X16D2	8 or less per one point
		32-point connector type, 24V DC	FP2–X32D2	4.3 or less per one point
		64-point connector type, 24V DC	FP2–X64D2	4.3 or less per one point
Output unit	Relay output	6-point terminal type	FP2–Y6R	70 or less
		16-point terminal type	FP2–Y16R	160 or less
	Transistor output	16-point terminal NPN type	FP2–Y16T	120 or less
		32-point connector NPN type	FP2–Y32T	140 or less
		64-point connector NPN type	FP2–Y64T	250 or less
		16-point terminal PNP type	FP2–Y16P	70 or less
		32-point connector PNP type	FP2–Y32P	150 or less
		64-point connector PNP type	FP2–Y64P	270 or less
I/O mixed unit	32-point 24V DC input/32-point connector NPN output type		FP2–XY64D2T, FP2–XY64D7T	Input: 4.3 or less per one point
				Output: 120 or less
	32-point 24V DC input/32-point connector PNP output type		FP2–XY64D2P, FP2–XY64D7P	Input: 4.3 or less per one point
				Output: 130 or less

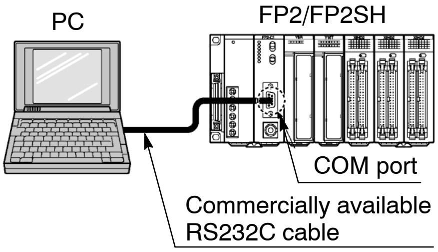
Notes

- **The input unit displays the current flowing to the internal circuit. The other units display the current value required to drive the internal circuit. This value does not include the load current of the output unit.**
- **Refer to the manual of the particular unit you are using to confirm the current consumed at 24V by the S-LINK units, Positioning units, High–speed counter units and Pulse I/O units.**

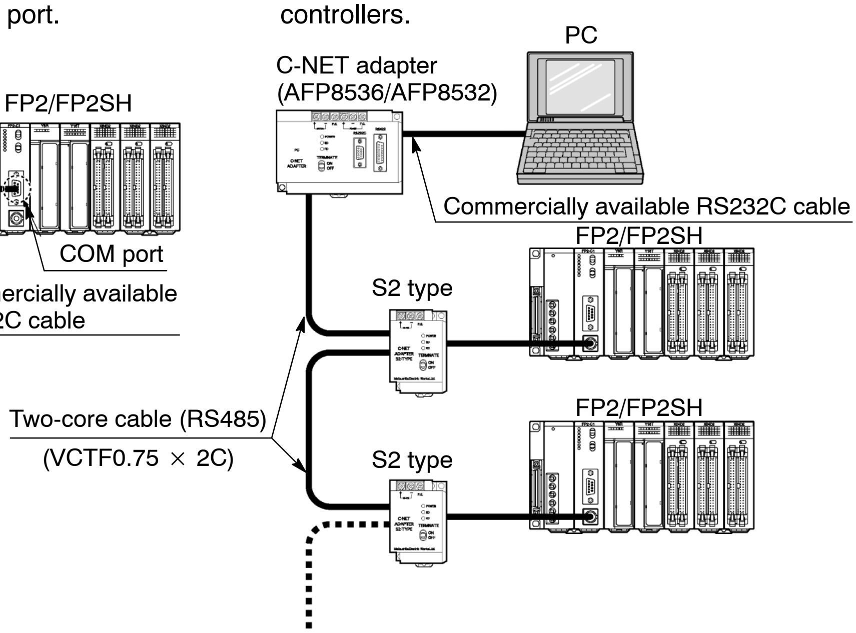
1.3 Expansion Function

1.3.1 Computer Link

1:1 communication
The FP2 CPU can be directly connected to a computer through the COM (RS232C) port.



1:N communication
A C-NET adapter can be used to enable communication for a number of programmable controllers.



A maximum of 32 stations can be connected.

Since a COM (RS232C) port and TOOL (RS232C) port comes standard on the CPU for the FP2/FP2SH, direct communication with the computer can be achieved without the addition of any intelligent units.

Using a host computer program, the relay conditions and register contents of the CPU can be read and written.

With communications from a host computer, communication programs are unnecessary on the CPU side.

Table of specifications

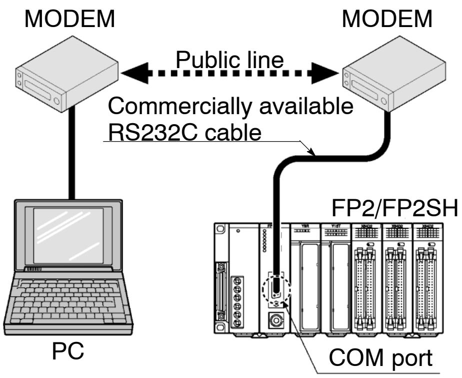
Item	Description	
	1:1 communication	1:N communication
Communication method	Half duplex	Half duplex
Synchronization method	Start–stop synchronous system	
Communication path	RS232C cable	Two-core cable (VCTF 0.75mm^2 × 2C)
Transmission distance	Max. 15m/49.2ft.	Max. 1200m/3,937ft.
Transmission speed (Baud rate)	1200bps/2400bps/4800bps/9600bps/ 19200bps/38400bps/57600bps/115.2Kbps	9600bps/19200bps
Transmission code	ASCII	
Transmission format	Stop bit: 1 bit/2 bits Parity check: none/even/odd Character bits: 7 bits/8 bits	

Necessary devices in configuration

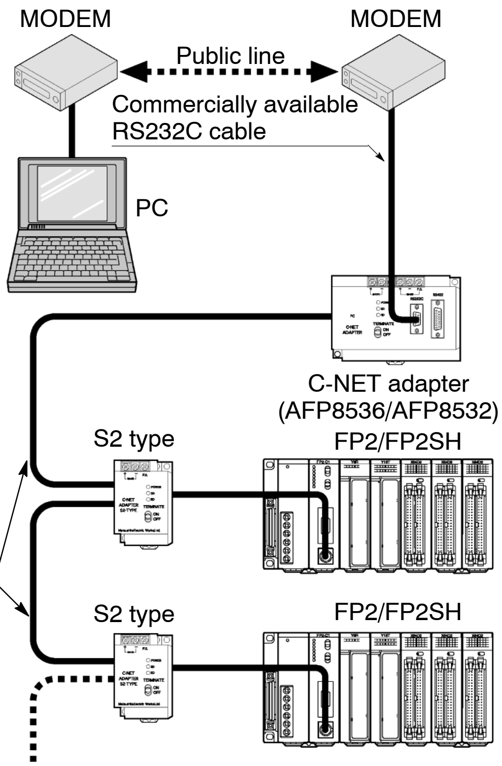
1:1 communication	1:N communication
FP2/FP2SH Commercially available computer Commercially available RS232C cable (AFB85813/AFB85853 or equivalent)	FP2/FP2SH Commercially available computer Commercially available RS232C cable (AFB85813/AFB85853 or equivalent) C-NET adapter (AFP8536/AFP8532) × 1 piece C-NET adapter S2 type (AFP15402) × number of PLC Two-core cable (VCTF 0.75mm^2)

1.3.2 Connection of MODEM

1:1 communication
Connections to a MODEM can be made using the COM port.



1:N communication
Using the C-NET adapter enables MODEMs to be connected for multiple programmable controller.



A maximum of 32 stations can be connected.

The CPU of the FP2/FP2SH includes a COM (RS232C) port and TOOL (RS232C) port as standard equipment, making it possible to connect a MODEM to perform programming and computer linking from a remote location using a public telephone line.

When the power supply of FP2/FP2SH is turned on, it will verify whether a MODEM is connected, and, if a MODEM is, it will automatically transmit the AT command to set the MODEM for automatic reception.

Since the reading and writing of the relay conditions and register contents of the programmable controller can be performed from the host computer, this function is applicable for remote monitoring systems.

When using the TOOL port, you can use programming tool software (NPST-GR/FPWIN GR) and perform reading and writing of the programmable controller program and maintenance operations via MODEM.

During 1:1 communication using the COM port, an error alarm can be issued from the programmable controller.

Table of specifications

Item	Description	
	1:1 communication	1:N communication
Communication method	Half duplex	
Synchronization method	Start–stop synchronous system	
Transmission speed (Baud rate)	2,400bps/4,800bps/9,600bps/19,200 bps	9,600bps/19,200bps
Transmission code	ASCII	
Transmission format	Character bit: 7 bits, parity check: odd and stop bit: 1 bit Character bit: 8 bits, parity check: none and stop bit: 1 bit	

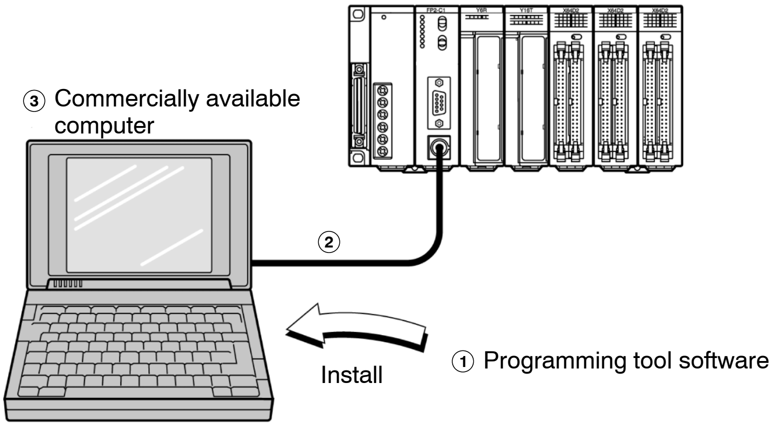
Necessary devices in configuration

1:1 communication	1:N communication
FP2/FP2SH	FP2/FP2SH
Commercially available computer	Commercially available computer
MODEM	MODEM
Commercially available RS232C cable	Commercially available RS232C cable
* When using the TOOL port, an FP PC cable M5 type (AFC8513) and a self-made cable are necessary.	C-NET adapter (AFP8536/AFP8532) × 1 piece
	C-NET adapter S2 type (AFP15402) × number of PLC
	Two-core cable (VCTF 0.75mm^2)

1.4 Programming Tools

1.4.1 Tools Needed for Programming

Necessary tools



① **Programming tool software**

This is a program editing, debugging and document creating software package that can be used with all programmable controllers in the FP series.

② **FP PC cable**

This cable needed for connection between the FP2/FP2SH and the computer.

When connecting to a computer (IBM PC/AT or 100% compatible), use a commercially available adapter.(☛ section 1.4.2)

For the following, use commercially available products.

③ **Commercially available computer**

1.4.2 Software Environment and Suitable Cable

Standard ladder diagram tool software FPWIN−GR Ver.2

Type of software		OS (Operating system)	Hard disk capacity	Product No.
FPWIN GR Ver. 2 English−language menu	Full type	Windows® 98 Windows® Me Windows® 2000 Windows® XP Windows Vista®	40MB or more	AFPS10520
	Upgraded version			AFPS10520R

Note

1) **Ver.1.1 must be installed to install the upgrade version.**
2) **Ver.2.0 can be upgraded to Ver. 2.1 or later free of charge at our web site (http://industrial.panasonic.com/ac/e/dl_center/software/).**

Conforms to IEC61131−3 programming tool software FPWIN−Pro Ver.6

Type of software	OS (Operating system)	Hard disk capacity	Product No.
FPWIN GR Ver. 6 English−language menu	Windows® 2000 Windows® XP Windows Vista®	100MB or more	AFPS50560

Note

1) **The upgrade version is not available for Ver.6.**
2) **Ver.6.0 can be upgraded to Ver. 6.1 or later free of charge at our web site (http://industrial.panasonic.com/ac/e/dl_center/software/).**

Type of computer and suitable cable
For the connection between a computer (RS232C) and the control unit (RS232C)
D−sub connector cable

PC side connector	PLC side connector	Specifications	Product No.
D−sub 9−pin	Mini DIN round 5−pin	L type (3 m)	AFC8503
	Mini DIN round 5−pin	Straight type (3 m)	AFC8503S

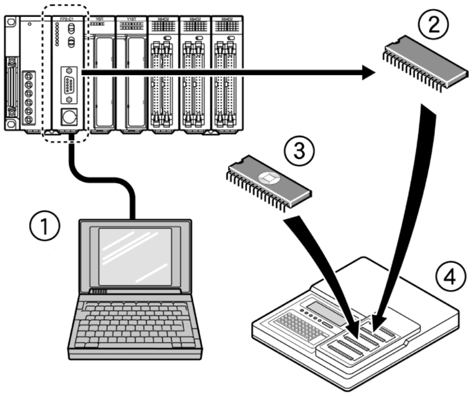
Note

A USB/RS232C conversion cable is necessary to connect with a personal computer without a RS232C port using a PC connection cable.

1.4.3 Tools Needed for ROM Creating

When Creating ROM with a Commercially Available ROM Writer with Optional Memory (FROM)

Necessary tools



① **Programming tool software and cable (☛ section 1.4.1)**
Use a commercially available computer installed with the programming tool software and an FP PC cable.

② **Optional memory FROM**
For FP2, FP2-EM4 (SST−29EE010−120−4C−PH or equivalent, SILICOM STORAGE TECHNOLOGY, INC.)
For FP2SH, AFP5208 (SST−29EE020−150−4C−PH or equivalent, SILICOM STORAGE TECHNOLOGY, INC.)

③ **Optional memory EPROM**
For FP2, FP2-EM5 (M27C1001−12F1 or equivalent, SGS−THOMSON MICROELECTRONICS)
For FP2SH, AFP5209 (M27C2001−150F1 or equivalent, SGS−THOMSON MICROELECTRONICS)

For the following, use commercially available products.

④ **Commercially available ROM writer**
A ROM writer than can be used with memories ② and ③.

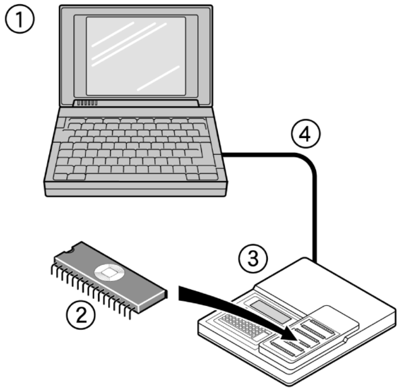
☞ **Note**

1) The above explanation describes the case where the memory unit is used in combination with the F−ROM and EP−ROM. As the nonvolatile memory has been implemented in the memory unit (Model number AFP2208), a commercial ROM writer cannot be used for writing.

2) The parts for the optional memory to be used differ depending on FP2 or FP2SH.

When Creating ROM with Programming Tool Software and a Commercially Available ROM Writer

Necessary tools



① **Programming tool software (☛ section 1.4.1)**
Use a commercially available PC installed with the programming tool software.

② **Optional memory EPROM**
For FP2, FP2-EM5 (M27C1001−12F1 or equivalent, SGS−THOMSON MICROELECTRONICS)
For FP2SH, AFP5209 (M27C2001−150F1 or equivalent, SGS−THOMSON MICROELECTRONICS)

For the following, use commercially available products.

③ **Commercially available ROM writer**
A ROM writer than can be used with memory ②.

④ **Commercially available centronics cable or commercially available RS232C cable**
Use a cable that conforms with the specifications of the ROM writer.

☞ **Note**

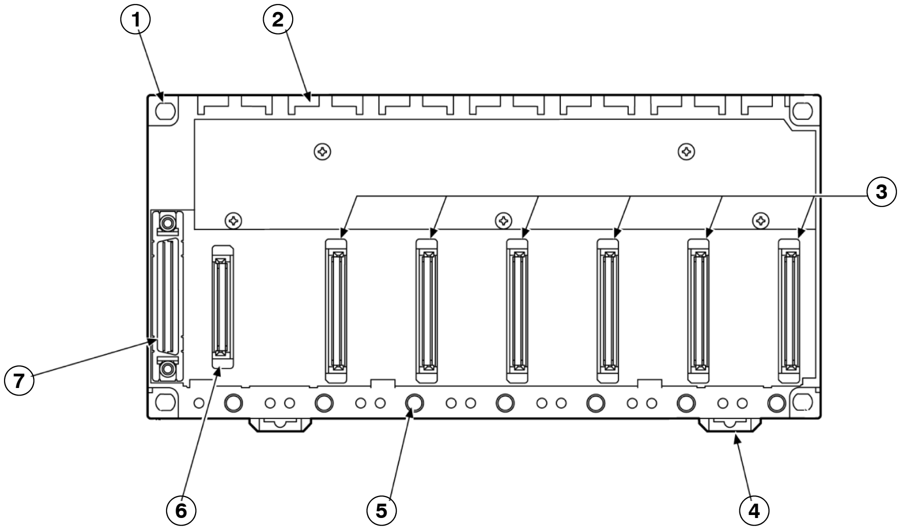
1) **The above explanation describes the case where the memory unit is used in combination with the EP−ROM. As the nonvolatile memory has been implemented in the memory unit (Model number AFP2208), a commercial ROM writer cannot be used for writing.**
2) **The parts for the optional memory to be used differ depending on FP2 or FP2SH.**

Chapter 2

Parts and Functions

2.1 Backplane and Expansion Cable

2.1.1 Backplane



Parts Terminology and Functions

① **Backplane mounting holes**
for mounting the backplane to the control panel. Use M4 screw for the mounting.

② **Unit guides**
Align the tab on the unit with this guide when installing the unit to the backplane.
For use as the basic backplane (CPU backplane), from the left side of the backplane, install the power supply unit, CPU, I/O units, and intelligent units, in this order.
For use as an expansion backplane, from the left side of the backplane, install the power supply unit, I/O units, and intelligent units, in this order.

③ **Connector for various units**
Install a CPU, input, or output unit. When installing a CPU, be sure to install it next to a power supply unit.

④ **DIN rail attachment lever**
allows attachment to a DIN rail.

⑤ **Unit installation holes**
for installing the unit to the backplane. Use the screw supplied with the unit for installation.

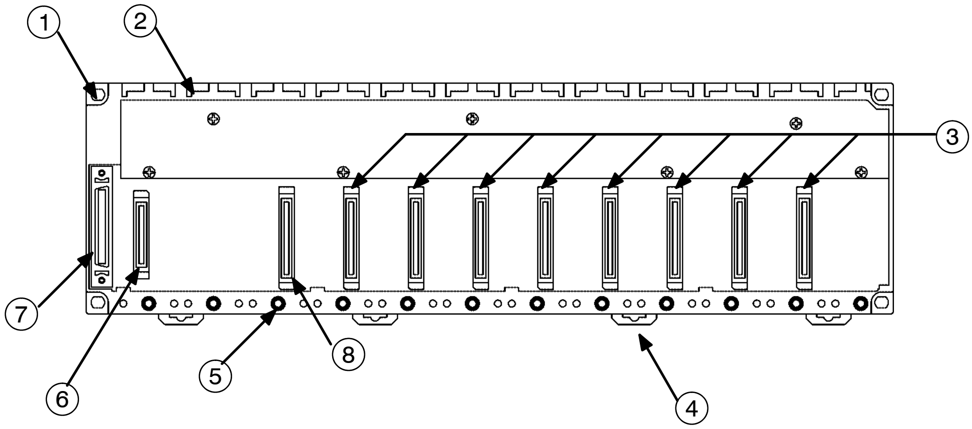
⑥ **Connector for power supply unit**

⑦ **Connector for expansion cable**
for more details regarding the cable connecting, refer to section 4.1.3.
This connector is not present on a 5-module type backplane.

Type of Backplane

Type	Use	Number of module	Part number	Weight
5-module type	Basic system only	5	FP2−BP05	Approx. 180g
7-module type	Basic and expansion system	7	FP2−BP07	Approx. 280g
9-module type		9	FP2−BP09	Approx. 350g
12-module type		12	FP2−BP12	Approx. 470g
14-module type		14	FP2−BP14	Approx. 530g

2.1.2 Basic Backplane H Type (FP2−BP**MH)



Parts Terminology and Functions

① **Backplane mounting holes**
for mounting the backplane to the control panel. Use M4 screw for the mounting.

② **Unit guides**
Align the tab on the unit with this guide when installing the unit to the backplane. From the left side of the backplane, install the power supply unit, CPU, I/O units, and intelligent units, in this order.

③ **Connector for various units**
Install various unit.

④ **DIN rail attachment lever**
allows attachment to a DIN rail.

⑤ **Unit installation holes**
for installing the unit to the backplane. Use the screw supplied with the unit for installation.

⑥ **Connector for power supply unit**

⑦ **Connector for expansion cable**
for more details regarding the cable connecting, refer to section 4.1.3.

⑧ **Connector for CPU unit**
The position to install the CPU unit is fixed.

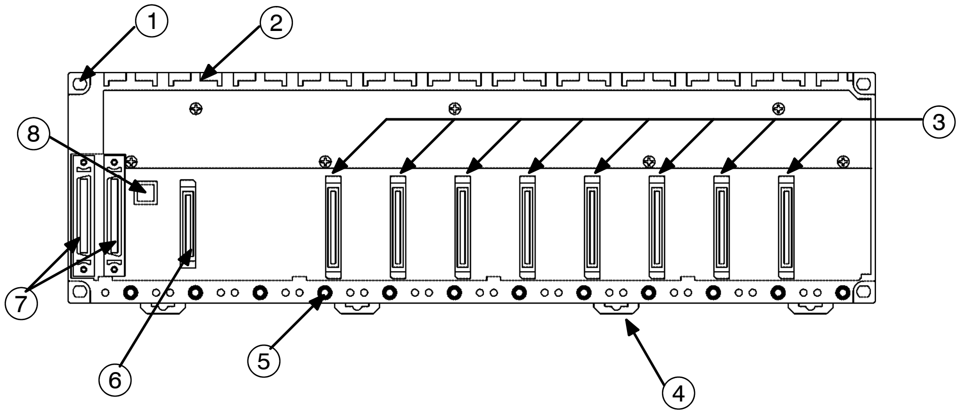
Type of Backplane

Type	Use	Number of module	Part number	Weight
11-module type	Basic system only	11	FP2−BP11MH	Approx. 470g

☞ **Note**

The color of letters on the printed board is yellow to make easier to distinguish the FP2 backplane H type from the FP2 backplane.

2.1.3 Expansion Backplane H Type (FP2−BP**EH)



Parts Terminology and Functions

① **Backplane mounting holes**
for mounting the backplane to the control panel. Use M4 screw for the mounting.

② **Unit guides**
Align the tab on the unit with this guide when installing the unit to the backplane. From the left side of the backplane, install the power supply unit, I/O units, and intelligent units, in this order.

③ **Connector for various units**
Install I/O unit.

④ **DIN rail attachment lever**
allows attachment to a DIN rail.

⑤ **Unit installation holes**
for installing the unit to the backplane. Use the screw supplied with the unit for installation.

⑥ **Connector for power supply unit**

⑦ **Connector for expansion cable**
for more details regarding the cable connecting, refer to section 4.1.3.

⑧ **Board number setting switch**
is used to set a bord number for the expansion backplane. I/O numbers are assigned according to the board number set the board numbers in increasing order, 1, 2 and 3 from the board close to the basic backplane.
(Do not set 4 or higher numbers as proper operation cannot be guaranteed).

Type of Backplane

Type	Use	Number of module	Part number	Weight
10-module type	Expansion system only	10	FP2−BP10EH	Approx. 470g

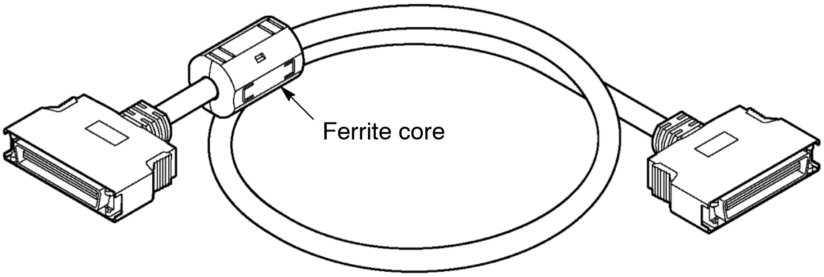
Note

The color of letters on the printed board is yellow to make easier to distinguish the FP2 backplane H type from the FP2 backplane.

2.1.4 Expansion Cable

Order number	Length	Ferrite core	Weight
FP2−EC	60 cm	1	Approx. 200 g
FP2−EC2	2 m	2	Approx. 400 g

Note) With the backplalne H type, the total cable length can be arranged within 3.2 m.

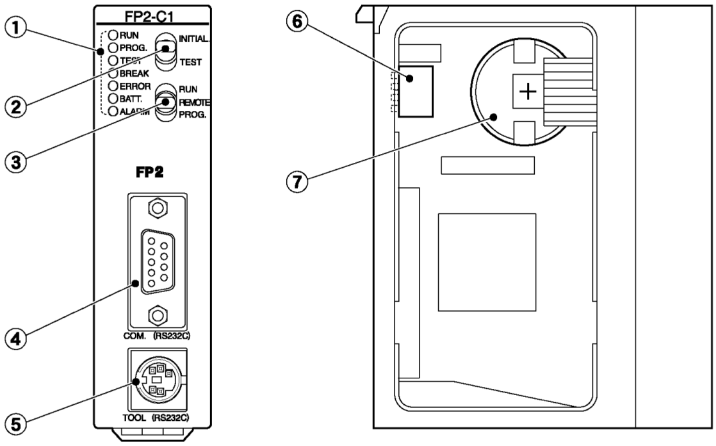


☞ Note

Connect the connector on the side of the ferrite core to the CPU backplane.

2.2 FP2 CPU

2.2.1 Standard Type CPU (FP2−C1)



Parts Terminology and Functions

① **Status indicator LEDs** (☛ page 2 – 9)
display the operating condition and error statuses.

② **Initialize/test switch** (☛ page 2 – 9)
is used to clear the errors, initializes the operation memory and set the test operation.

③ **Mode selector** (☛ page 2 – 10)
is used to change the operation mode of the PLC.

④ **COM port (RS232C)** (☛ page 2 – 11)
is used to connect a computer or general−serial devices.

⑤ **Tool port (RS232C)**
is used to connect a programming tool.

⑥ **Operation condition switches** (☛ page 2 – 10)
are used to set the baud rate of the programming tool, to select the program memory and to select the writing operation for the program memory.

⑦ **Memory backup battery**
for backup of the internal memory (RAM).
Part number: AFC8801 (CR2450 or equivalent)

Note

The settings of the operation condition switches become active when the power is turned on.

Status Indicator LEDs

These LEDs display the current mode of operatin or the occurrence of error.

LED	Description
RUN (green)	This lights in the RUN mode, to indicate that the program is being executed. It flashes during forced input/output.
PROG. (green)	This lights in the PROG. mode. Operation stops while this LED is lighted. It flashes when waiting for connection of slave station on remote I/O system. If the memory is initialized, the brightness dims, indicating that initialization is being executed.
TEST (green)	This lights in the test operation mode.
BREAK (green)	This lights in the operation halts at a break during a test run or halts during the step operation mode for the test run.
ERROR (red)	This lights if an error is detected during the self-diagnostic function.
BATT. (red)	This lights when the voltage of the backup battery drops below a specific value.
ALARM (red)	This lights if a hardware error occurs, or if operation slows because of the program, and the watchdog timer is activated.

Initialize/Test Switch

This switch clears errors, initializes the operation memory and sets the test operation mode.

Switch position	Operation mode
INITIALIZE (upward)	**In the PROG. mode:** The contents of the operation memory are initialized. However, the system register (including the I/O map) and the program are not initialized. If the error of self-diagnostic error code 42 or lower is occured, the special internal relays R9000 to R9008 and the special data register DT90000 are not cleared. **In the RUN mode:** Operation errors, remote I/O system errors, and battery errors are cleared.
(center)	The switch should normally be left in this position.
TEST (downward)	Setting this switch to the downward position in the PROG. mode, accesses the test mode. Switching to the RUN mode in this state, initiates test operation. To return from the test mode to the normal operation, return this switch to the center position in the PROG. mode.

☞ **Note**

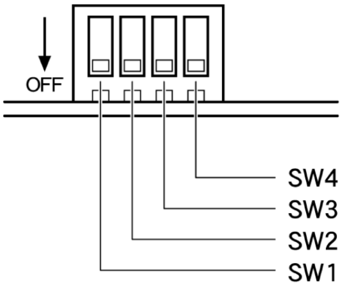
By turning on the initialize/test switch while in the PROG.mode, you can be specify the type of operation memory to be cleared with system register 4.

Mode Selector

Use the mode selector to start and stop the operation. For test operations, set the initialize/test switch to TEST position.

Selector position	Operation mode
RUN (upward)	This sets the RUN mode. The program is executed, and operation begins.
REMOTE (center)	This enables operation to be started and stopped from a programming tool. At the stage where the selector is changed, when switching from the PROG. to the REMOTE mode, the system remains in the PROG. mode and when switching from the RUN to the REMOTE mode, it remains in the RUN mode.
PROG. (downward)	This sets the PROG. mode. In this mode, programming can be done using tools, the test operation mode can be accessed and the operation memory can be initialized using the Initialize/tset switch.

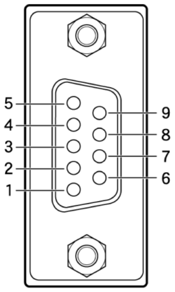
Operation Condition Switches



Switch	Item	Switch position	
		off (factory setting)	on
SW1	Baud rate for tool port	System register setting (Default value: 19,200bps)	9,600bps
SW2	Program memory selection	Internal RAM	Optional memory (ROM)
SW3	Program memory protection	Write enabled	Write protected
SW4	Not used	—	—

COM Port (RS232C)

Pin alignment



Pin number	Signal name		Signal direction	
			PLC	Destination (Field device)
1	Frame ground	FG		
2	Send data	SD	→	
3	Received data	RD	←	
4	Request to send (always on)	RS	→	
5	Clear to send	CS	←	
6	Not used	–		
7	Signal ground terminal	SG		
8	Not used	–		
9	Equipment ready (always on)	ER	→	

☞ **Note**

The serial data communication control instruction (F144) cannot be executed unless pin 5 is turned on.

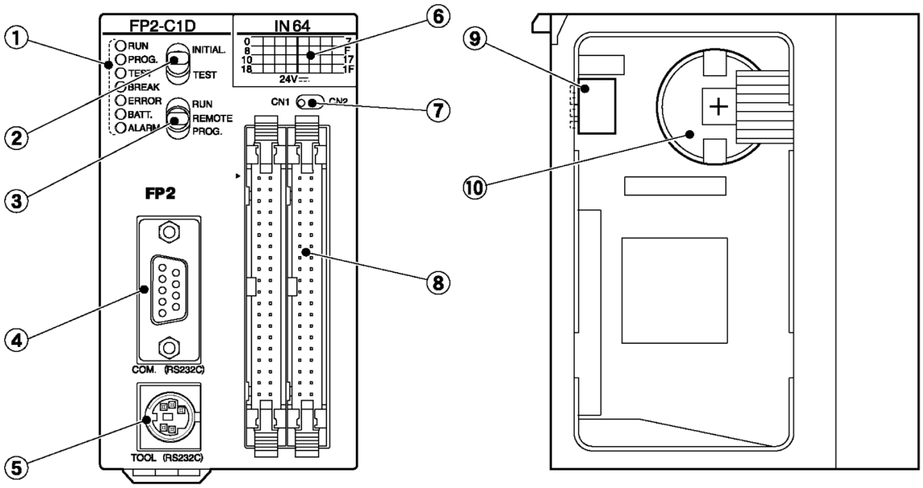
Communications specifications

Electrical characteristics conform to EIA RS232C.
The baud rate and transmission format are decided by system registers.
The table below shows the settings in the default state.

Item	Description
Mode selection Computer link Baud rate	19200 bps
Data bit length	8 bits
Parity check	Odd parity
Start bit length	1 bit
Stop bit length	1 bit

The starting and ending codes when using a computer link are determined by the MEW-TOCOL–COM.
When using the general–purpose communication function (serial data communication control instruction “F144”), the setting of system register 412 should be changed.
The serial data communication control instruction can be used to switch between the computer link function and the general–purpose communication function.
If the transmission speed is 38,400 bps or higher, the transmission distance over which communication is possible is limited to within 3m/9.84ft.

2.2.2 CPU with 64 Points Input (FP2–C1D)



Parts Terminology and Functions

① **Status indicator LEDs** (☛ page 2 – 9)
display the operating condition and error statuses.

② **Initialize/test switch** (☛ page 2 – 9)
is used to clear the errors, initializes the operation memory and set the test operation.

③ **Mode selector** (☛ page 2 – 10)
is used to change the operation mode of the PLC.

④ **COM port (RS232C)** (☛ page 2 – 11)
is used to connect a computer or general–serial devices.

⑤ **Tool port (RS232C)**
is used to connect a programming tool.

⑥ **Input indicators (32 points)**
Indicate the input on/off states.

⑦ **Selector for input indicators**
switch between the first 32 points and second 32 points of the 64 points input LED display.

⑧ **Input connectors**
CN1: X0 to X1F
CN2: X20 to X3F

⑨ **Operation condition switches** (☛ page 2 – 10)
are used to set the baud rate of the programming tool, to select the program memory and to select the writing operation for the program memory.

☛ next page

⑩ **Memory backup battery**
for backup of the internal memory (RAM).
Part number: AFC8801 (CR2450 or equivalent)

Note

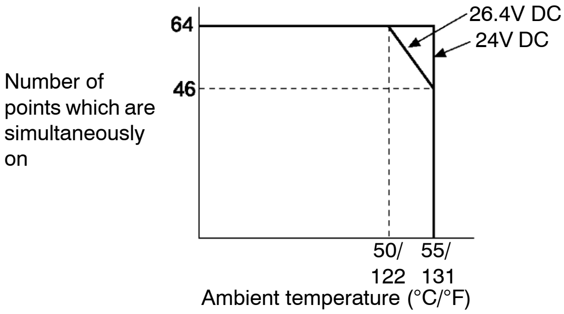
The settings of the operation condition switches become active when the power is turned on.

CPU with 64 Points Input Specifications

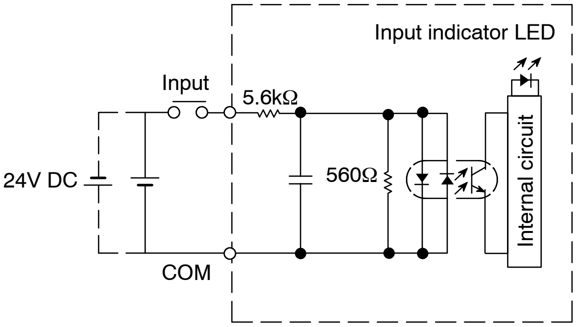
Item		Description
Number of input point		64 points
Insulation method		Optical coupler
Rated input voltage		24V DC
Rated input current		Approx. 4.3mA (at 24V DC)
Input impedance		Approx. 5.6kΩ
Input voltage range		20.4 to 26.4V DC
Min. on voltage/Min. on current		19.2V/4mA
Max. off voltage/Max. off current		5.0V/1.5mA
Response time	off → on	0.2ms or less
	on → off	0.3ms or less
Input points per common		32 points per common (Either the positive or negative of the input power supply can be connected to common terminal.)
Operating indicator		32-dot LED display (lit when on, switching)
External connection method		Two 40-pin connectors

Note

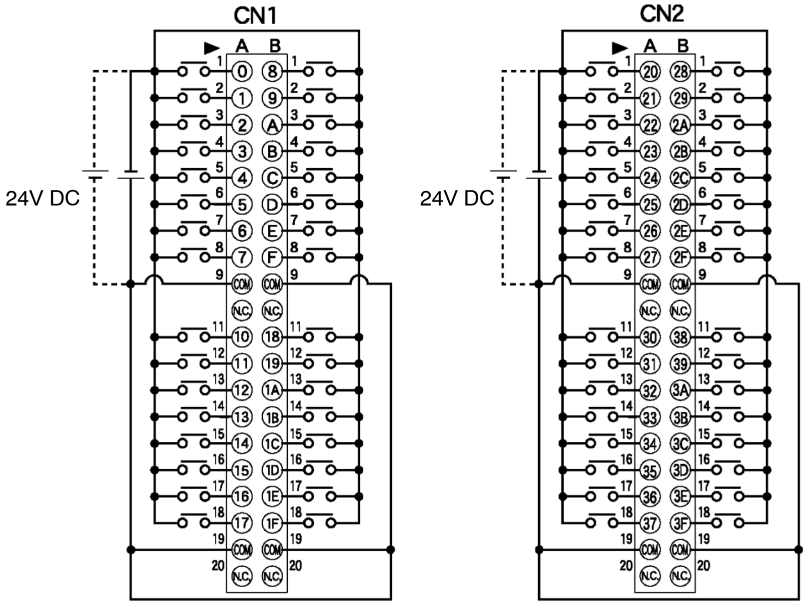
Keep the number of input points which are simultaneously on within the following range as determined by the input voltage and ambient temperature.



Internal Circuit Diagram



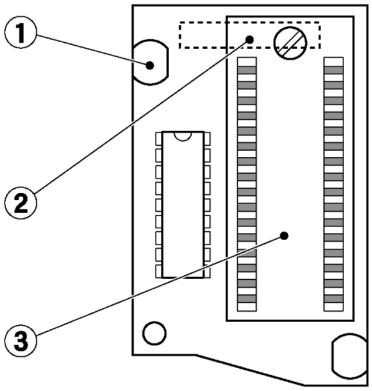
Pin Layout



The COM pins of each connector are connected internally.

2.3 Expansion Memory Unit and ROM (for FP2 CPU)

Expansion Memory Unit



Parts Terminology

① **Mounting knob**

② **Connector (rear side)**

③ **ROM IC socket (for FP2−EM3, FP2−EM6 and FP2−EM7)**
Install the optional memory FROM or EPROM.

Type of Expansion Memory Unit

Item	Part number					Description
	FP2−EM1	FP2−EM2	FP2−EM3	FP2−EM6	FP2−EM7	
Comment input function (flash ROM)	Available 128k byte	Available 128k byte	Available 512k byte	Not available	Not available	Writes the I/O comments, remarks and block comments in the program to the FP2 CPU.
Calendar/ timer function	Available	Available	Available	Not available	Not available	Allows operations using the calendar/timer function.
Expansion RAM	Not available	Available	Available	Available	Not available	Increases the program memory from approx. 16K to approx. 32K. Also enables use of the trace function.
ROM IC socket	Not available	Not available	Available	Available	Available	Enables the program to be copied to ROM for ROM operation.

Type of ROM

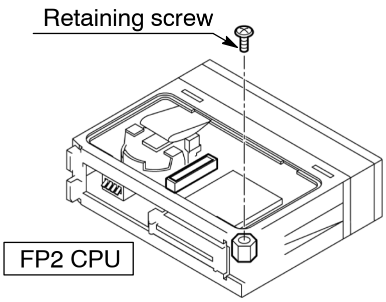
Type	Description	Part number
FROM	Equivalent to the 29EE010−120−4C−PH (SILICON STORAGE TECHNOLOGY, INC.). Enables writing with the operation of the programming tools when attached to the CPU.	FP2−EM4
EPROM	Equivalent to the M27C1001−12F1 (SGS-THOMSON MICROELECTRONICS). A commercially available ROM writer is required for writing.	FP2−EM5

Installation Procedure

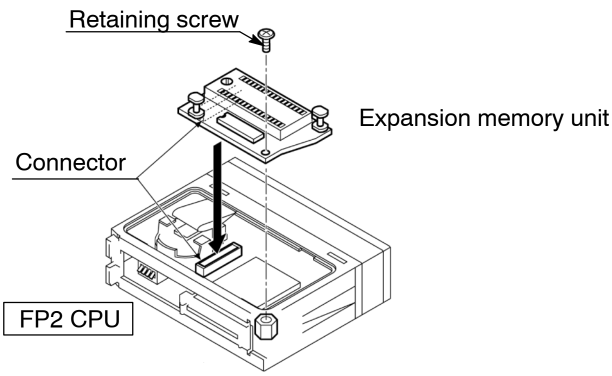
Installing the expansion memory unit

Procedure:

1. Send the program and data to the personal computer using the programming tool software (NPST−GR or FPWIN GR).
2. Save the program and data to the disk.
3. Set the mode selector of the FP2 CPU to PROG.
4. Turn off the power supply and remove the FP2 CPU.
5. Remove the retaining screw.



6. Install the expansion memory unit.
7. Secure the expansion memory unit with the retaining screw.



8. Install the FP2 CPU to the backplane and turn on the power supply.
9. Perform a program clear using the programming tool software.
10. Send to the FP2 CPU the program and data saved in step 2 above.

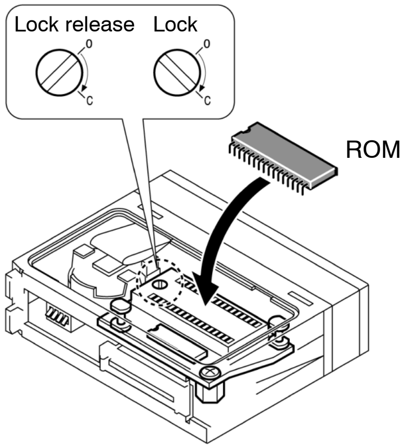
(For the FP2−EM2, FP2−EM3 and FP2−EM6, continue with the procedures below.)

11. At the “NPST Configuration” menu for NPST−GR or “Select PLC Type” menu for FPWIN GR of programming tool software, set the PLC type to FP2(32K).
12. Set the program capacity with system register 0.

Installing the ROM

Procedure:

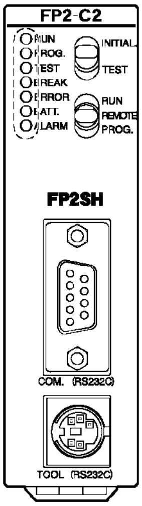
1. Release the lock for the ROM IC socket.
2. Make sure that the lead pitch of the ROM matches that of the socket.
3. Making sure that the orientation is correct, insert the ROM into the socket.
4. Return the lock to the locked position completely after the ROM is inserted.



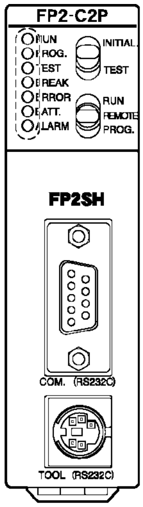
☞ Note

When removing or installing the expansion memory unit, the contents of the internal RAM may be erased. Therefore, always save the program onto a disk before beginning the removal and installation operations. During the installation or removal operations, do not touch the leads on any of the IC with your hands.

2.4 FP2SH CPU



Standard type CPU

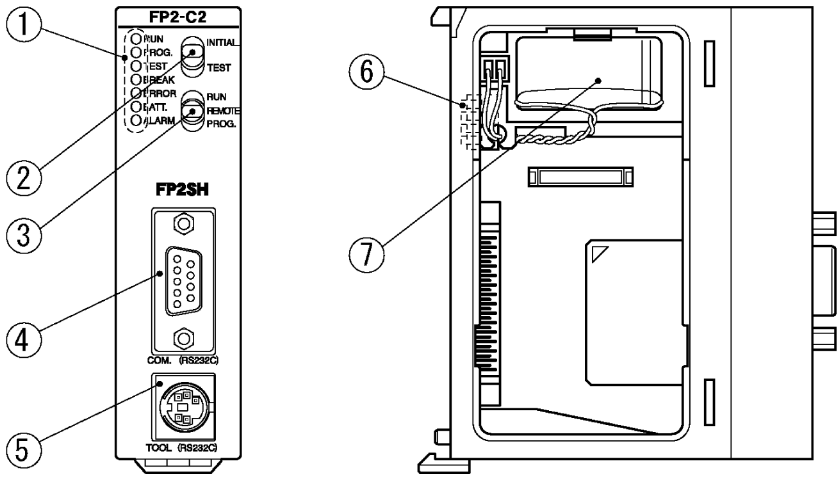


Small PC card
compliant type CPU

Type of FP2SH CPU

Type	Operation speed	Internal RAM	Optional memory			Function		Part number	Model number
			Expansion RAM	ROM	IC card	Calendar/ timer	Comment memory		
32k steps Standard type CPU	From 0.03μs	32k steps	Not available	Available (Optional)	Not available	Available (Built-in)	Available (Built-in)	FP2-C2L	AFP2221
60k steps Standard type CPU		60k steps	Not available	Available (Optional)	Not available	Available (Built-in)	Available (Built-in)	FP2-C2	AFP2231
60k steps CPU with IC memory card interface		60k steps	Not available	Available (Built-in)	Available (Optional)	Available (Built-in)	Available (Built-in)	FP2-C2P	AFP2235
120k steps CPU with IC memory card inter-face		120k steps	Not available	Available (Built-in)	Available (Optional)	Available (Built-in)	Available (Built-in)	FP2-C3P	AFP2255

2.4.1 32k/60k Step Standard Type CPU (FP2-C2L/FP2-C2)



Parts Terminology and Functions

① **Status indicator LEDs** (☛ page 2 – 9)
display the operating condition and error statuses.

② **Initialize/test switch** (☛ page 2 – 9)
Setting the switch to the ”INITIAL” side clears errors and initializes the operation memory. Setting the switch to the ”TEST” side puts the PLC in the test operation mode.

③ **Mode selector** (☛ page 2 – 10)
is used to change the operation mode of the PLC.
This is used to switch between the RUN, REMOTE, and PROG. modes.

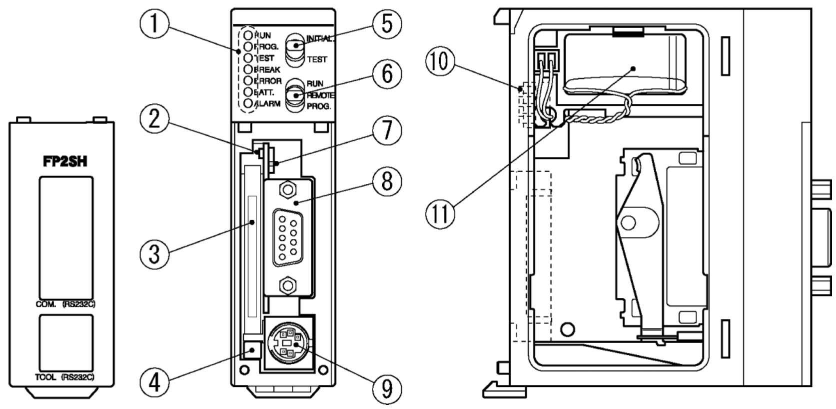
④ **COM port (RS232C)** (☛ page 2 – 11)
is used to connect a computer or general–serial devices .

⑤ **Tool port (RS232C)**
is used to connect a programming tool.

⑥ **Operation condition switches** (☛ page 2 – 21)
are used to set the baud rate of the programming tool, to select the program memory and to select the writing operation for the program memory.

⑦ **Memory backup battery**
for backup of the internal memory (RAM).
Part number: AFC8801 (CR2450 or equivalent)

2.4.2 CPU with IC Memory Card Interface (FP2-C2P/FP2–C3P)



Parts Terminology and Functions

① **Status indicator LEDs** (☛ page 2 – 9)
display the operating condition and error statuses.

② **IC memory card access LED**
Illuminates when data is being read from or written to the IC memory card.

③ **IC memory card slot**
is used when installing an optional IC memory card.

④ **IC memory card eject button**
Pressing this button ejects the IC memory card.

⑤ **Initialize/test switch** (☛ page 2 – 9)
Setting the switch to the “INITIAL” side clears errors and initializes the operation memory. Setting the switch to the “TEST” side puts the PLC in the test operation mode.

⑥ **Mode selector** (☛ page 2 – 10)
is used to change the operation mode of the PLC.
This is used to switch between the RUN, REMOTE, and PROG. modes.

⑦ **IC memory card access enable switch**
Setting this switch to the “on” (upward) side enables data to be read and written to the IC memory card.

⑧ **COM port (RS232C)** (☛ page 2 – 11)
is used to connect a computer or general–serial devices .

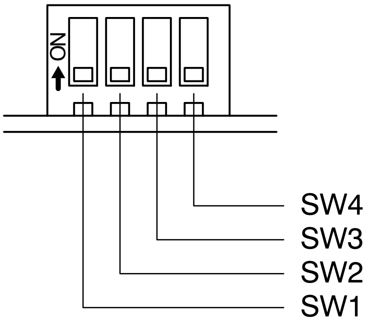
⑨ **Tool port (RS232C)**
is used to connect a programming tool.

☛ next page

⑩ **Operation condition switches**
are used to set the baud rate of the programming tool, to select the program memory and to select the writing operation for the program memory.

⑪ **Memory backup battery**
for backup of the internal memory (RAM).
Part number: AFC8801 (CR2450 or equivalent)

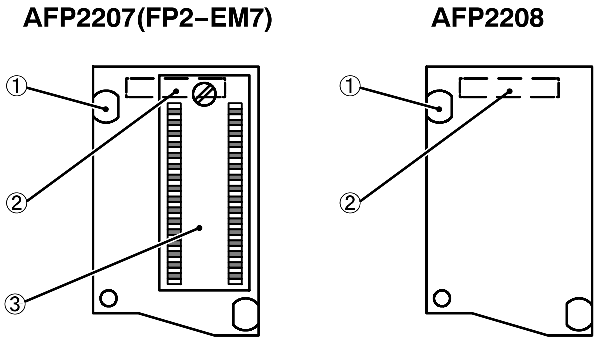
Operation Condition Switches



Switch	Item	Switch position	
		off (factory setting)	on
SW1	Baud rate for tool port	System register setting (Default value: 19,200bps)	9,600bps
SW2	Program memory selection	Internal RAM	External memory
SW3	Program memory protection	Write enabled	Write protected
SW4	External memory selection	ROM	IC memory card

2.5 Expansion Memory Unit and ROM (for FP2−C2L/FP2-C2)

Parts Terminology



① **Mounting knob**

② **Connector (rear side)**

③ **ROM IC socket**
Install the optional memory FROM or EPROM.

Type of Expansion Memory Unit

Type	Function	Part number	Model number
Expansion memory unit	Socket for installing the ROM in the CPU	FP2−EM7	AFP2207
	Nonvolatile memory−implemented memory unit	—	AFP2208

Note

The FP2−EM1, FP2−EM2, FP2−EM3, and FP2−EM6 expansion memory units for the FP2 cannot be used.
As for the memory unit AFP2208, the ROM is not removable.

Type of ROM

Type	Function	Part number
FROM	Equivalent to the 29EE020−150−4C−PH (SILICON STORAGE TECHNOLOGY, INC.). Enables writing with the operation of the programming tools when attached to the CPU.	AFP5208
EPROM	Equivalent to the M27C2001−150F1 (SGS-THOMSON MICROELECTRONICS). A commercially available ROM writer is required for writing.	AFP5209

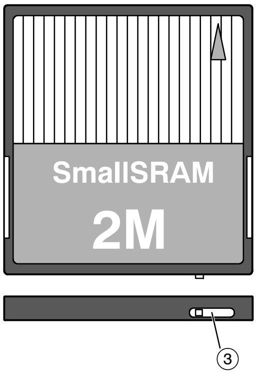
Installation Procedure

For detailed information about the installation of expansion memory unit ☛ page 2 – 16

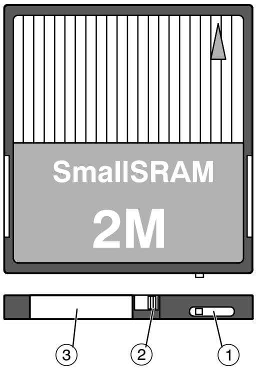
For detailed information about the installation of ROM ☛ page 2 – 17

2.6 IC Memory Card (for FP2-C2P/FP2-C3P)

AIC50020, AIC52000

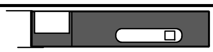
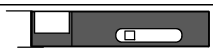


AFP2209



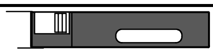
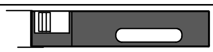
Parts and Functions

① Write protect switch

Switch position		Purpose
	**ON (right)**	Read−only of the data
	**OFF (left)**	Write enable of the data

② Lock switch

It fixes the battery holder.

Switch position		Purpose
	**LOCK (right)**	Lock position
	**RELEASE (left)**	Release position

Note) The lock switch is automatically back to the LOCK position from the RELEASE position when removing the battery holder.

③ Battery holder

A battery for memory backup is installed. (A battery is supplied with the product.)
Product number for purchasing separately: AFP2806

Role of IC Memory Card

The IC memory card can be used as a memory to which programs can be saved and copied, or as an expanded memory to which data can be read and written in the program.

The IC memory card can be divided into two areas, a “format field” in which various programs are stored, and an “expanded memory field” used as a data memory.

Example:

A 2MB card can be formatted as 1 MB, with 1 MB being used as a “format field” and the remaining 1 MB being used as an “expanded memory field”.

The entire field can be used as a “format field” or as an “expanded memory field”, and the card used exclusively as a memory card for saving programs or data memory.

If the FROM section is specified as the “expanded memory field”, the card can be used only for reading data.

Types of IC Memory Cards

Type	Memory capacity	Part number	Usage method		Recommended application points
			When used to store programs	When used as expanded memory field	
FROM type	2 MB	AIC50020	Data is written to IC memory card using “Copy File to IC Card” of programming tool software.	Serves as dedicated memory for reading data. Data is written using programming tool software. Data is read from IC memory card using high−level instruction **F12 (ICRD)**.	No battery back-up is required, so this is ideal for saving programs.
SRAM type **SRAM type**	2 MB	AFP2209 AIC52000 (Discontinued products)	Programs are written to IC memory card using “Download Program to IC Card” of programming tool software. Programs can be written from internal RAM to IC memory card using “ROM ← RAM” of programming tool software.	Writing of data to IC memory card is done using high−level instruction **F13 (ICWT)**. Reading of data from IC memory card is done using high−level instruction **F12 (ICRD)**.	Data can be read to and written from programs, so this is ideal for use as expansion data memory.

Notes

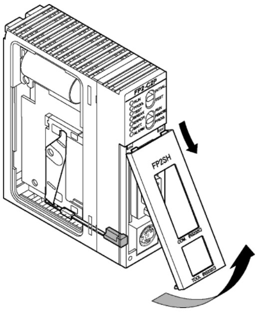
- **Both the SRAM and FROM type can be divided into a “format field” and an “expanded memory field” for use.**
- **When using the card as a program memory, there are four ways to read programs:**
  - **Programs are read automatically when the power is turned on (IC memory card operation).**
  - **Programs are read using the “ROM → RAM” operation of programming tool software.**
  - **Programs are read using the “IC Card Service” of programming tool software.**
  - **Programs are read using the F14 (PGRD) instruction of the sequence program.**

Inserting and Removing the IC Memory Card

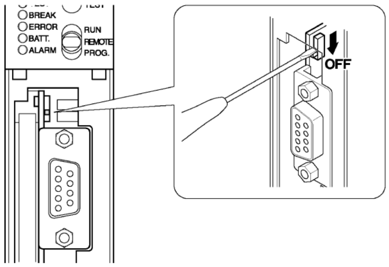
The IC memory card can be inserted or removed even when the FP2SH power is on. To insert or remove the card when the power is on, be sure to follow the following procedure.

Inserting procedure:

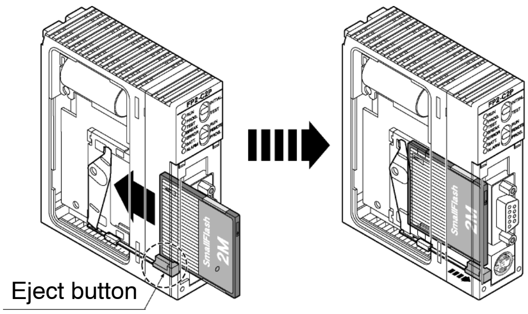
1. **Remove the cover of FP2SH CPU.**



2. **Set the IC memory card access enable switch to off position.**



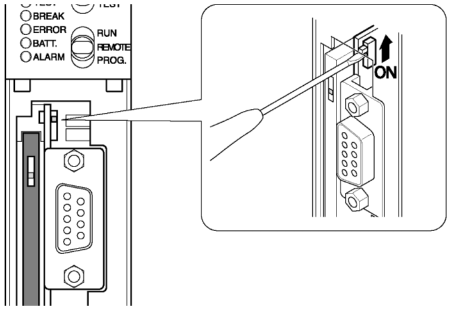
3. **Insert the IC memory card.**



☞ **Note**

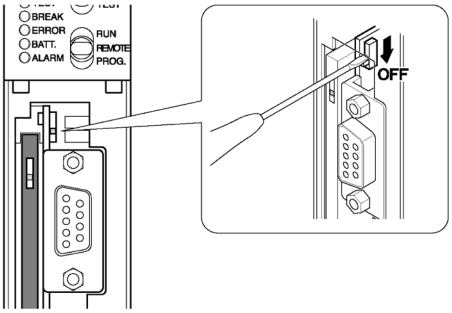
When using AFP2209, confirm if the battery is installed in the IC memory card.

4. **Set the IC memory card access enable switch to on position.**

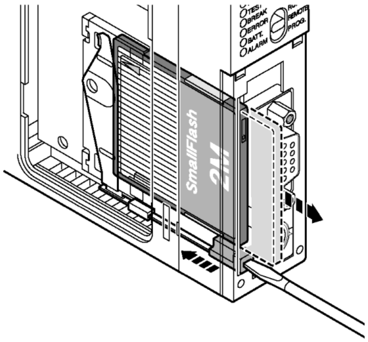


Removal procedure:

1. **Verify that the IC memory card access LED is off. Set the IC memory card access enable switch to off position.**



2. **Push the eject button and pull out the IC memory card.**



Precautions when installing/removing the IC memory card

Do not try to insert and remove the IC memory card while the IC memory card access enable switch is on. It could lead to damage of the memory contents or a malfunction of CPU.

Do not use excessive force to the card or the section where card is installed.

Battery of the SRAM type IC memory card

AIC52000

A rechargeable battery is used. It cannot be exchanged.

AFP2209

An interchangeable battery is used. When you use for the first time, install the battery included.

☞ Note

If the battery voltage has dropped, the ERROR LED lights, and error code K55 or K54 is stored in special data register DT90000. Error codes can be confirmed using programming tools.

K54 -- The data on the IC memory card is not retained.

K55 -- The data on the IC memory card is guaranteed, but the voltage of the internal battery has dropped.

***AIC52000: Power should continue to be supplied to the unit in order to charge it.**

***AFP2209: The replacement of memory backup battery is neces sary. As the data saved in AFP2209 is overwritten when replacing the battery, the data must be backed up before the replacement.**

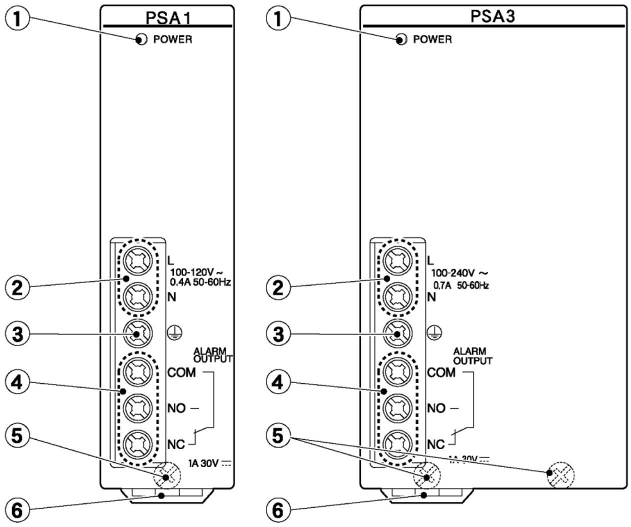
Write protection of IC memory card

There is a write protect switch on the IC memory card. To prohibit writing to the IC memory card, set this switch to “Write protect” position.

To write the program or data to the IC memory card, set the write protect switch to off position.

2.7 Power Supply Units

2.7.1 Power Supply Specifications



Parts Terminology and Functions

① **POWER LED**

Turns on when power is applied.

② **Power supply terminal**

is the terminal for power supply wiring. Uses M3 crimping (pressure connection) terminals (☛ section 4.2.1).

③ **Ground terminal**

To minimize effects from noise and prevent electrical shocks, connect this terminal to ground.

④ **Alarm output terminal**

Contact output terminals of the relay which turns on when the ALARM LED of the CPU turns on. Normally closed contact (N.C.) and normally open contact (N.O.) are available.

⑤ **Unit installation screw**

⑥ **Temporary holding hook**

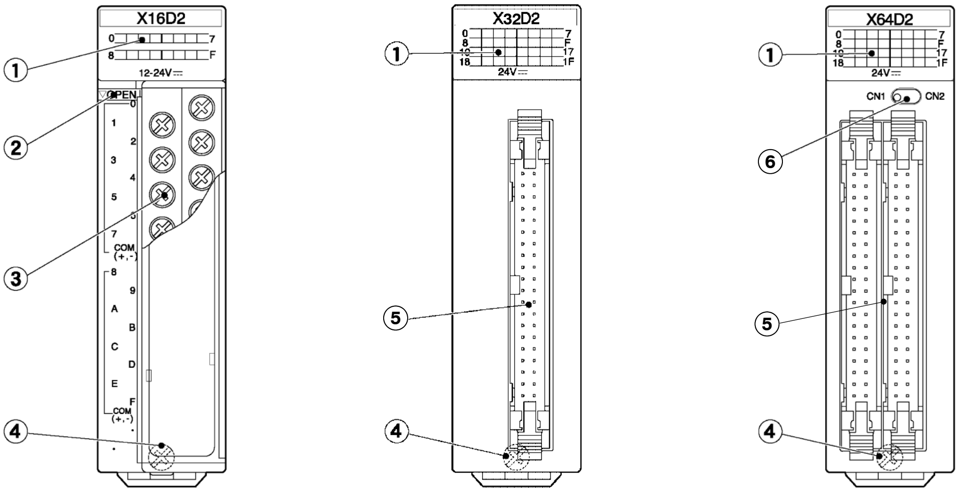
Specifications

Item		Description			
Part number		FP2−PSA1	FP2−PSA2	FP2−PSA3	FP2−PSD2
Size of unit		1−module		2−module	
Input	**Rated voltage**	100 to 120V AC	200 to 240V AC	100 to 240V AC	24V DC
	Current consumption	0.4A or less (at 100V AC)	0.2A or less (at 200V AC)	0.7A or less (at 100V AC) 0.4A or less (at 200V AC)	2.5A or less
	Surge current	40A or less		30A or less (at 25°C/77°F)	10A or less
	Rated frequency	50Hz/60Hz			—
	Operating voltage range	85 to 132V AC	170 to 264V AC	85 to 264V AC	20.4 to 31.2V DC (*1)
Output	**Output capacity at 5V**	Max. 2.5A		Max. 5A	Max. 5A
Alarm contact capacity		30V DC 1A			
Alarm contact operation		When the ALARM LED of CPU is lit			
Alarm contact type		1c contact			
Leakage current		Between input and ground terminals, 0.75mA or less			
Breakdown voltage		1500V AC for 1 minutes (between input and ground terminals)			500V AC for 1 minutes (between input and ground terminals)
Insulation resistance		100MΩ 500V DC (between input and ground terminals)			
Guaranteed lifetime		20000 hours at 55°C/131°F			
Overcurrent protection function		Built-in overcurrent protection			
Fuse		Built-in			
Terminal screw		M3			

*1 The allowable variation in voltage after startup is 15.6V to 31.2V.

2.8 Input and Output Units

2.8.1 Common Specifications of Input and Output Units



Parts Terminology and Functions

① **Input and output indicators**

Indicate the input and output on/off states.

② **Terminal block release lever**

By lowering this lever, the terminal block can be removed from the unit without removing any of the wiring. After installation, push in the lock button at the bottom of the unit to lock in the terminal block.

③ **Terminal block**

This is the terminal block for the inputs, outputs, and power supplies. This terminal block uses M3 sized crimping (pressure connection) terminals. For more information regarding the crimping (pressure connection) terminals, refer to section 4.5.1.

④ **Unit installation screw**

Secures the unit to the backplane.

⑤ **Connector**

This is the connector for input/output and power supply wiring. This allows the connector of discrete-wire and the connector of flat cable. For more information regarding the suitable connectors, refer to section 4.4.1.
For terminal connection, an exclusive cable is available. For more information, refer to section 4.4.3.

⑥ **Indicator selection switch**

Switches between the first 32 points (CN1 position) and second 32 points (CN2 position) of the LED display for the 64-point type unit.

Table of Input Unit Types

Type	Number of points	Connection method	Description	Part number
DC input type	16 points	Terminal block	12 to 24V DC, sink/source input	FP2–X16D2
	32 points	Connector	24V DC, sink/source input	FP2–X32D2
	64 points	Connector	24V DC, sink/source input	FP2–X64D2

Table of Output Unit Types

Type	Number of points	Connection method	Description	Part number
Relay output type	6 points	Terminal block	5A, Without relay sockets	FP2–Y6R
	16 points	Terminal block	2A, Without relay sockets	FP2–Y16R
Transistor (NPN open collector) output type	16 points	Terminal block	5 to 24V DC, 0.5A	FP2–Y16T
	32 points	Connector	5 to 24V DC, 0.1A	FP2–Y32T
	64 points	Connector	5 to 24V DC, 0.1A	FP2–Y64T
Transistor (PNP open collector) output type	16 points	Terminal block	5 to 24V DC, 0.5A	FP2–Y16P
	32 points	Connector	5 to 24V DC, 0.1A	FP2–Y32P
	64 points	Connector	5 to 24V DC, 0.1A	FP2–Y64P

☞ **Note**

The maximum load current for the transistor output type output unit will differ depending on the operating voltage.
Refer to the specifications pages for each unit.

Table of I/O Mixed Unit Types

Type	Number of points	Connection method	Description	Part number
DC input/transistor (NPN open collector) output type	32 input points/ 32 output points	Connector	24V DC, sink/source input, 5 to 24V DC, 0.1A	FP2−XY64D2T
DC input/transistor (PNP open collector) output type	32 input points/ 32 output points	Connector	24V DC, sink/source input, 5 to 24V DC, 0.1A	FP2−XY64D2P
DC input with on pulse catch input function/transistor (NPN open collector) output type	32 input points/ 32 output points	Connector	24V DC, sink/source input, 5 to 24V DC, 0.1A	FP2−XY64D7T
DC input with on pulse catch input function/transistor (PNP open collector) output type	32 input points/ 32 output points	Connector	24V DC, sink/source input, 5 to 24V DC, 0.1A	FP2−XY64D7P

Notes

- **The maximum load current value will differ depending on the operating voltage. Refer to the specifications page for each unit.**
- **For types with the on pulse catch input, the four points X1C through X1F of the 32 input points possess the on pulse catch input function. (☛ section 2.11.5)**

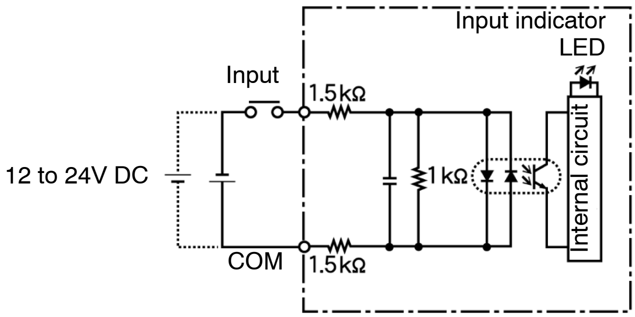
2.9 Input Units Specifications

2.9.1 16-point Type DC Input Unit

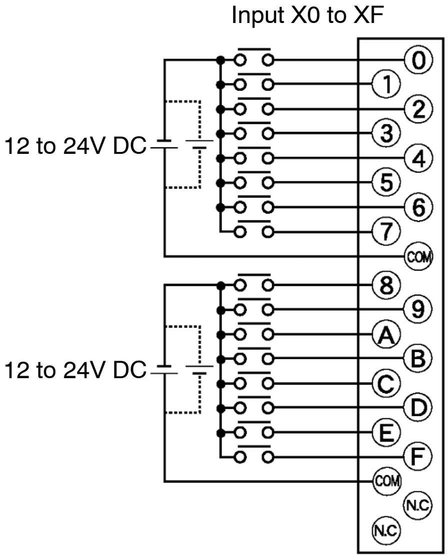
Specifications

Item		Description
Part number		FP2–X16D2
Insulation method		Optical coupler
Rated input voltage		12 to 24V DC
Rated input current		Approx. 8mA (at 24V DC)
Input impedance		Approx. 3kΩ
Input voltage range		10.2 to 26.4V DC (Max. input current: 10mA or less)
Min. on voltage/Min. on current		9.6V/4mA
Max. off voltage/Max. off current		2.5V/1mA
Response time	**off → on**	0.2ms or less
	on → off	0.2ms or less
Internal current consumption (at 5V DC)		60mA or less
Common method (Input points per common)		8 points/common Either the positive or negative of the input power supply can be connected to common terminal.
Operating indicator		16-dot LED display (lit when on)
External connection method		Terminal block (M 3 screw)
Weight		Approx. 140g

Internal Circuit Diagram



Pin Layout



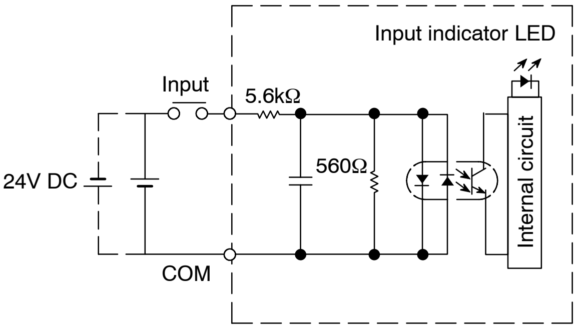
For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.1.

2.9.2 32-point Type DC Input Unit

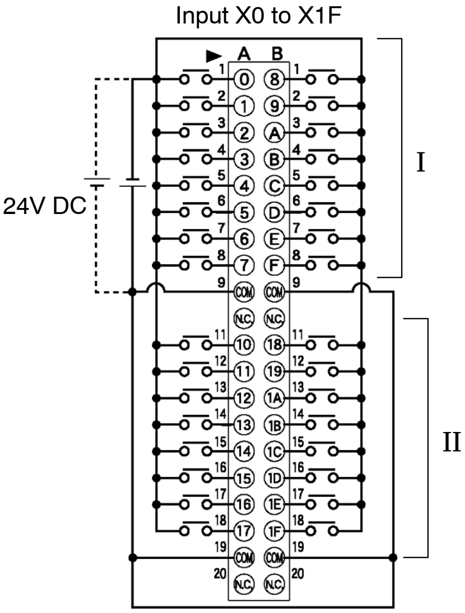
Specifications

Item		Description
Part number		FP2–X32D2
Insulation method		Optical coupler
Rated input voltage		24V DC
Rated input current		Approx. 4.3mA (at 24V DC)
Input impedance		Approx. 5.6kΩ
Input voltage range		20.4 to 26.4V DC
Min. on voltage/Min. on current		19.2V/4mA
Max. off voltage/Max. off current		5.0V/1.5mA
Response time	**off → on**	0.2ms or less
	on → off	0.3ms or less
Internal current consumption (at 5V DC)		80mA or less
Common method (Input points per common)		32 points/common Either the positive or negative of the input power supply can be connected to common terminal.
Operating indicator		32-dot LED display (lit when on)
External connection method		Connectors (MIL type 40-pin)
Weight		Approx. 100g

Internal Circuit Diagram



Pin Layout



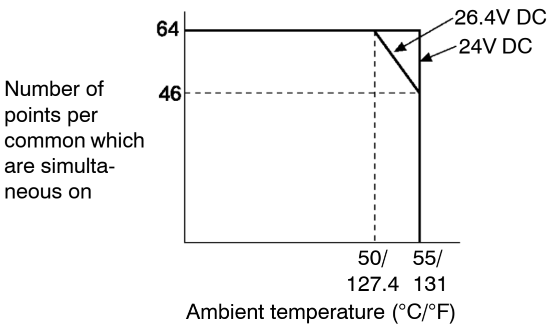
2.9.3 64-point Type DC Input Unit

Specifications

Item		Description
Part number		FP2–X64D2
Insulation method		Optical coupler
Rated input voltage		24V DC
Rated input current		Approx. 4.3mA (at 24V DC)
Input impedance		Approx. 5.6kΩ
Input voltage range		20.4 to 26.4V DC
Min. on voltage/Min. on current		19.2V/4mA
Max. off voltage/Max. off current		5.0V/1.5mA
Response time	**off → on**	0.2ms or less
	on → off	0.3ms or less
Internal current consumption (at 5V DC)		100mA or less
Common method (Input points per common)		32 points/common Either the positive or negative of the input power supply can be connected to common terminal.
Operating indicator		32-dot LED display (lit when on, switching)
External connection method		Connectors (MIL type two 40-pin)
Weight		Approx. 120g

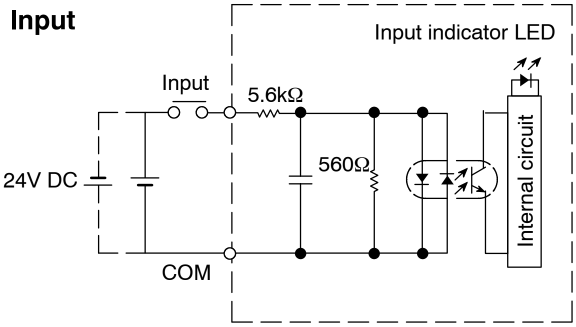
Note

Keep the number of input points per common which are simultaneously on within the following range as determined by the input voltage and ambient temperature.

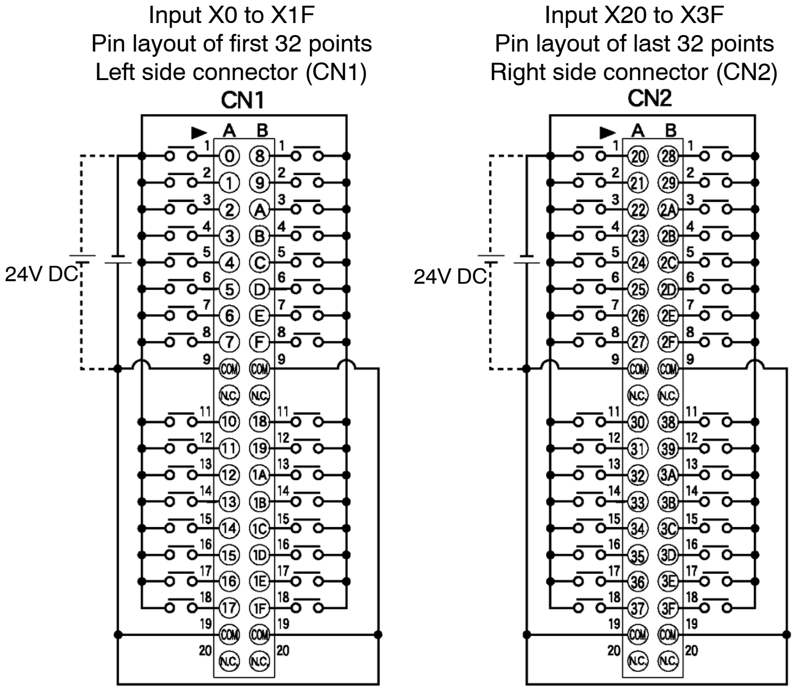


Internal Circuit Diagram

Input



Pin Layout



The COM pins of each connector are connected internally.

For more information regarding the applicable connectors and terminals, refer to section 4.4.1.

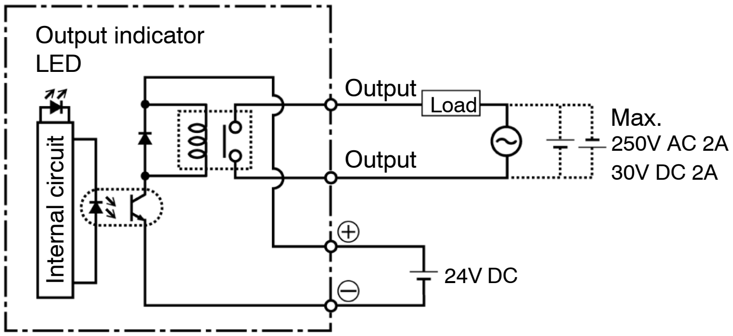
2.10 Output Units Specifications

2.10.1 16-point Type Relay Output Unit

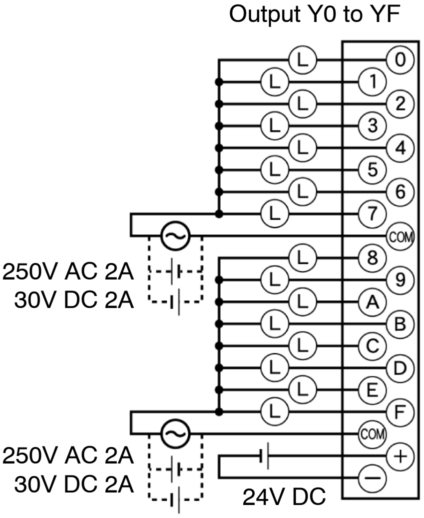
Specifications

Item		Description
Part number		FP2-Y16R
Insulation method		Optical coupler
Rated control capacity		2A 250V AC (5A/common), 2A 30V DC (5A/common) Min. load: 100μA, 100mV (resistor load)
Response time	**off → on**	10ms or less
	on → off	8ms or less
Life time	**Mechanical**	20,000,000 operations or more
	Electrical	100, 000 operations or more
Internal current consumption (at 5V DC)		120mA or less
Power supply for driving internal circuit	**Voltage**	24V DC ± 10% (21.6 to 26.4V DC)
	Current	160mA or less
Surge absorber		None
Relay socket		None
Common method (Output points per common)		8 points/common
Operating indicator		16-dot LED display (lit when on)
External connection method		Terminal block (M 3 screw)
Weight		Approx. 190g

Internal Circuit Diagram



Pin Layout



For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.1.

2.10.2 6-point Type Relay Output Unit

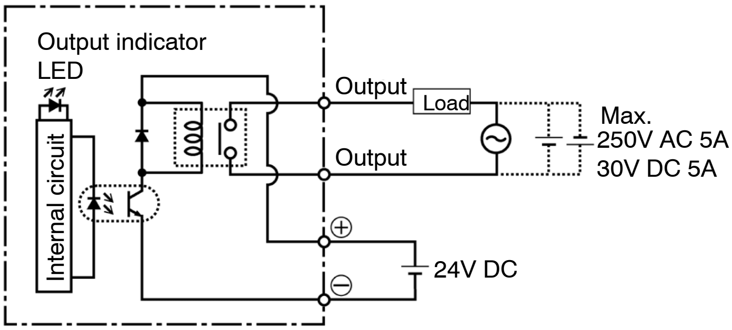
Specifications

Item		Description
Part number		FP2−Y6R
Insulation method		Optical coupler
Rated control capacity		5A 250V AC (10A/common), 5A 30V DC (10A/common)(* Note) Min. load: 100mA, 10V (resistor load)
Response time	**off → on**	10ms or less
	on → off	8ms or less
Life time	**Mechanical**	20,000,000 operations or more
	Electrical	100, 000 operations or more
Internal current consumption (at 5V DC)		50mA or less
Power supply for driving internal circuit	**Voltage**	24V DC ± 10% (21.6 to 26.4V DC)
	Current	70mA or less
Surge absorber		None
Relay socket		None
Common method (Output points per common)		2 points/common
Operating indicator		6-dot LED display (lit when on)
External connection method		Terminal block (M 3 screw)
Weight		Approx. 170g

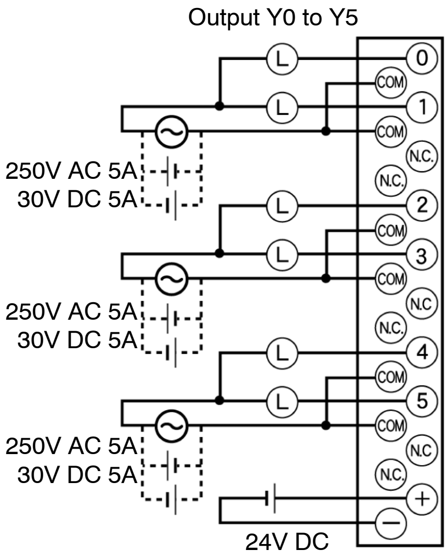
☞ **Note**

For each common 1 pin, use at a current capacity of 5A or less.

Internal Circuit Diagram



Pin Layout



For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.1.

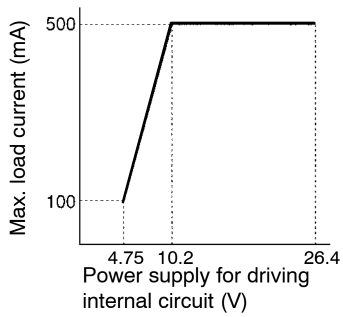
2.10.3 16-point Type Transistor (NPN) Output Unit

Specifications

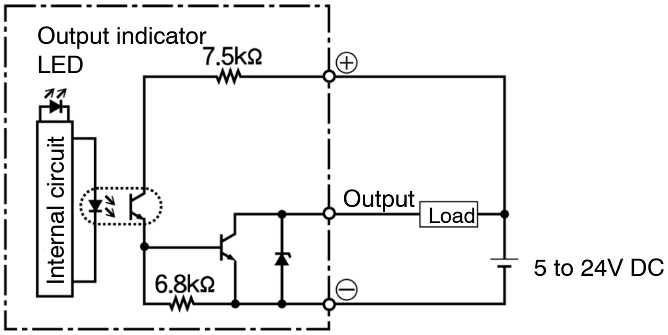
Item		Description
Part number		FP2–Y16T
Insulation method		Optical coupler
Rated load voltage		5 to 24V DC
Load voltage range		4.75 to 26.4V DC
Maximum load current		0.5A (at 12 to 24V DC), 0.1A (at 5V DC) (* Note)
Maximum surge current		3A, 10ms or less
Off state leakage current		1μA or less
On state maximum voltage drop		0.5V or less
Response time	**off → on**	0.1ms or less
	on → off	0.3ms or less
Internal current consumption (at 5V DC)		100mA or less
Power supply for driving internal circuit	**Voltage**	4.75 to 26.4V DC (* Note)
	Current	120mA or less (at 24V DC)
Surge absorber		Zener diode
Fuse ratings		None
Common method (Output points per common)		8 points/common
Operating indicator		16-dot LED display (lit when on)
External connection method		Terminal block (M 3 screw)
Weight		Approx. 150g

☞ **Note**

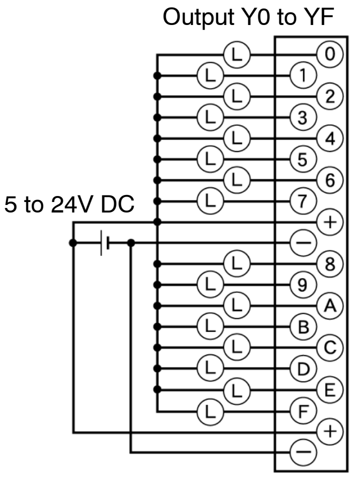
The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



Internal Circuit Diagram



Pin Layout



For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.1.

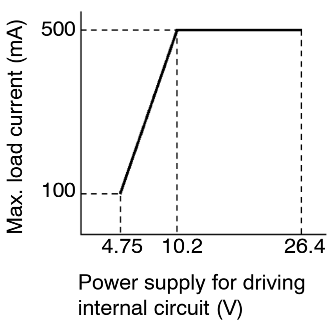
2.10.4 16-point Type Transistor (PNP) Output Unit

Specifications

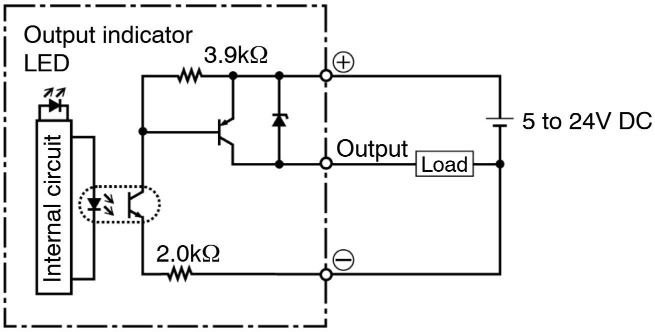
Item		Description
Part number		FP2−Y16P
Insulation method		Optical coupler
Rated load voltage		5 to 24V DC
Load voltage range		4.75 to 26.4V DC
Maximum load current		0.5A (at 12 to 24V DC), 0.1 A (at 5V DC) (* Note)
Maximum surge current		3A, 10ms or less
Off state leakage current		1μA or less
On state maximum voltage drop		0.5V or less
Response time	**off → on**	0.1ms or less
	on → off	0.3ms or less
Internal current consumption (at 5V DC)		80mA or less
Power supply for driving internal circuit	**Voltage**	4.75 to 26.4V DC (* Note)
	Current	70mA or less (at 24V DC)
Surge absorber		Zener diode
Fuse ratings		None
Common method (Output points per common)		8 points/common
Operating indicator		16-dot LED display (lit when on)
External connection method		Terminal block (M 3 screw)
Weight		Approx. 150g

☞ **Note**

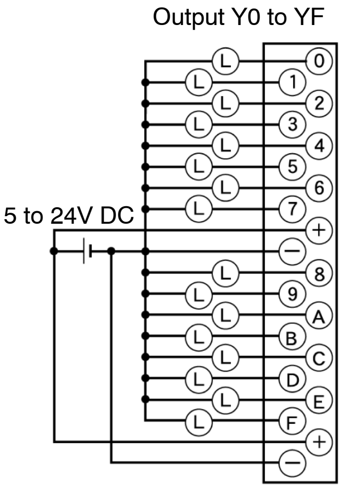
The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



Internal Circuit Diagram



Pin Layout



For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.1.

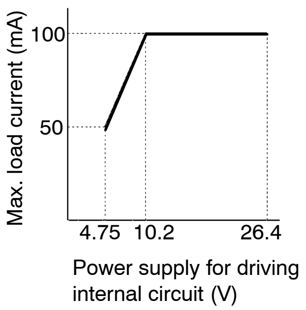
2.10.5 32-point Type Transistor (NPN) Output Unit

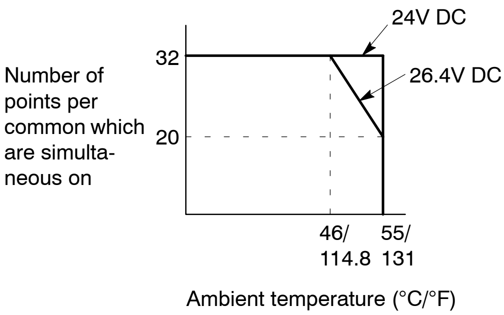
Specifications

Item		Description
Part number		FP2−Y32T
Insulation method		Optical coupler
Rated load voltage		5 to 24V DC
Load voltage range		4.75 to 26.4V DC
Maximum load current		0.1A (at 12 to 26.4V DC) , 50mA (at 5V DC) (* Note)
Maximum surge current		0.3A
off state leakage current		1μA or less
on state maximum voltage drop		1V or less (at 6 to 26.4V DC), 0.5V or less (at 6V DC or less)
Response time	off → on	0.1ms or less
	on → off	0.3ms or less
Internal current consumption (at 5V DC)		130mA or less
Power supply for driving internal circuit	Voltage	4.75 to 26.4V DC
	Current	140mA or less (at 24V DC)
Surge absorber		Zener diode
Fuse ratings		None
Common method (Output points per common)		32 points/common
Operating indicator		32-dot LED display (lit when on)
External connection method		Connector (MIL type 40-pin)
Weight		Approx. 100g

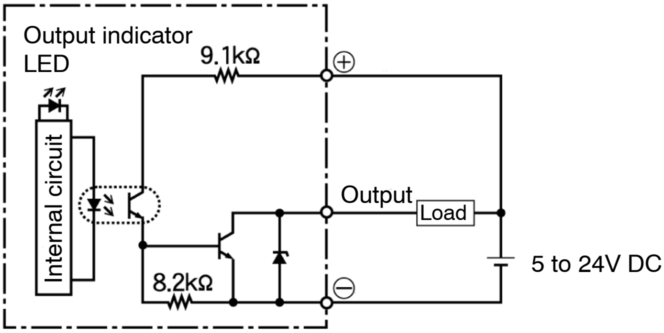
Note

The load current will vary depending on the power supply for driving the internal circuit and the ambient temperature. Adjust the load current referring to the following range.

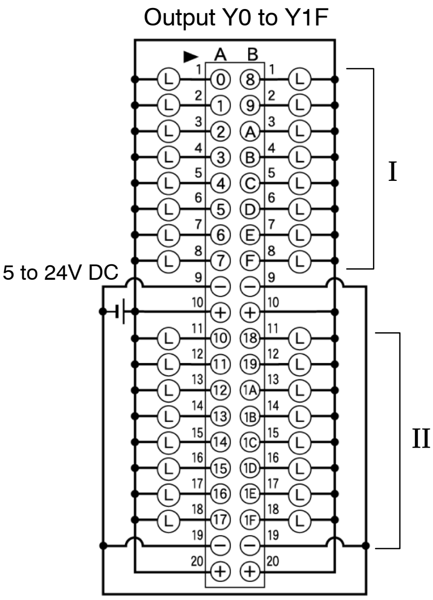




Internal Circuit Diagram



Pin Layout



Although ⊕ and ⊖ terminals are connected internally with the same connector. It is recommended that they also be connected externally.

For more information regarding the applicable connectors and terminals, refer to section 4.4.1.

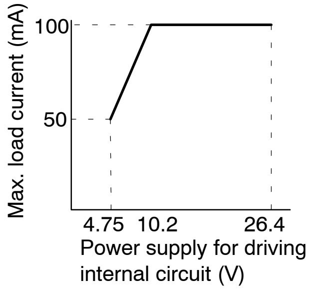
2.10.6 32-point Type Transistor (PNP) Output Unit

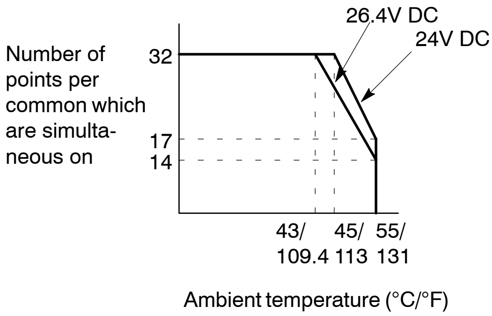
Specifications

Item		Description
Part number		FP2−Y32P
Insulation method		Optical coupler
Rated load voltage		5 to 24V DC
Load voltage range		4.75 to 26.4V DC
Maximum load current		0.1A (at 12 to 26.4V DC), 50mA (at 5V DC) (* Note)
Maximum surge current		0.3A
off state leakage current		1μA or less
on state maximum voltage drop		1.5V or less (at 6 to 26.4V DC), 0.5V or less (at 6V DC or less)
Response time	**off → on**	0.1ms or less
	on → off	0.3ms or less
Internal current consumption (at 5V DC)		130mA or less
Power supply for driving internal circuit	**Voltage**	4.75 to 26.4V DC
	Current	150mA or less (at 24V DC)
Surge absorber		Zener diode
Fuse ratings		None
Common method (Output points per common)		32 points/common
Operating indicator		32-dot LED display (lit when on)
External connection method		Connectors (MIL type 40-pin)
Weight		Approx. 100g

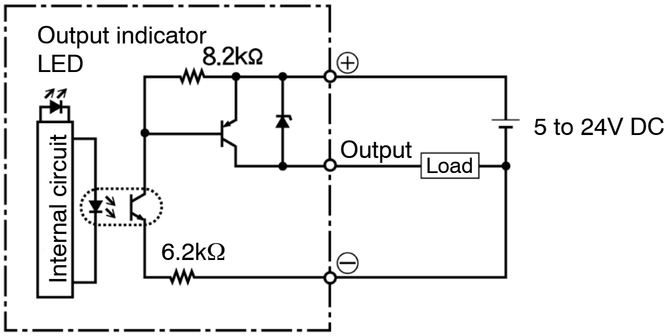
Note

The load current will vary depending on the power supply for driving the internal circuit and the ambient temperature. Adjust the load current referring to the following range.



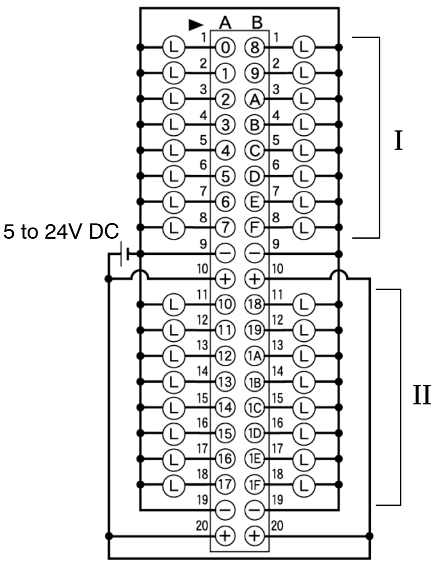


Internal Circuit Diagram



Pin Layout

Output Y0 to Y1F



Although ⊕ and ⊖ terminals are connected internally with the same connector. It is recommended that they also be connected externally.

For more information regarding the applicable connectors and terminals, refer to section 4.4.1.

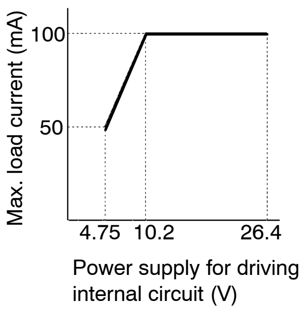
2.10.7 64-point Type Transistor (NPN) Output Unit

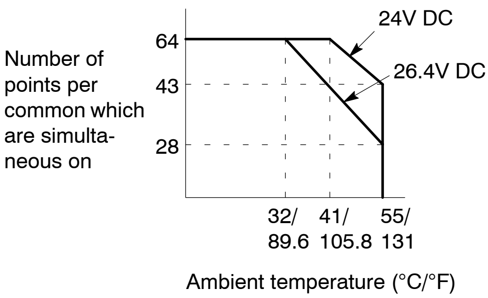
Specifications

Item		Description
Part number		FP2–Y64T
Insulation method		Optical coupler
Rated load voltage		5 to 24V DC
Load voltage range		4.75 to 26.4V DC
Maximum load current		0.1A (at 12 to 24V DC) , 50mA (at 5V DC) (* Note)
Maximum surge current		0.3A
Off state leakage current		1μA or less
On state maximum voltage drop		1V or less (at 6 to 26.4V DC), 0.5V or less (at 6V DC or less)
Response time	off → on	0.1ms or less
	on → off	0.3ms or less
Internal current consumption (at 5V DC)		210mA or less
Power supply for driving internal circuit	Voltage	4.75 to 26.4V DC
	Current	250mA or less (at 24V DC)
Surge absorber		Zener diode
Fuse ratings		None
Common method (Output points per common)		32 points/common
Operating indicator		32-dot LED display (lit when on, switching)
External connection method		Connector (MIL type two 40-pin)
Weight		Approx. 120g

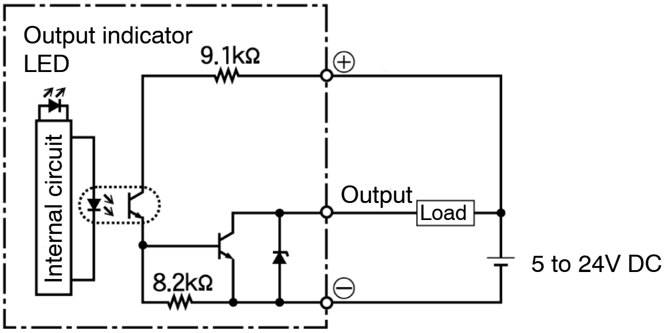
Note

The load current will vary depending on the power supply for driving the internal circuit and the ambient temperature. Adjust the load current referring to the following range.





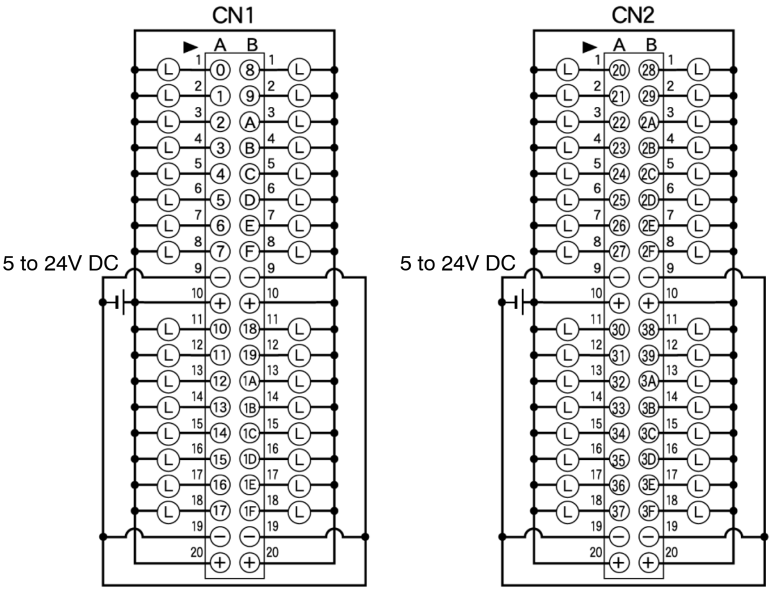
Internal Circuit Diagram



Pin Layout

Output Y0 to Y1F
Pin layout of first 32 points
Left side connector (CN1)

Output Y20 to Y3F
Pin layout of last 32 points
Right side connector (CN2)



Although ⊕ and ⊖ terminals are connected internally with the same connector. It is recommended that they also be connected externally.

For more information regarding the applicable connectors and terminals, refer to section 4.4.1.

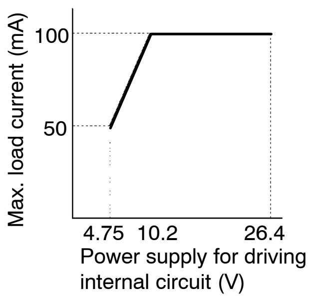
2.10.8 64-point Type Transistor (PNP) Output Unit

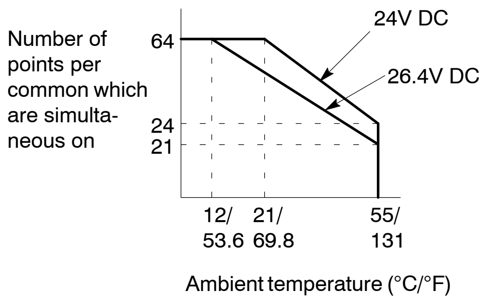
Specifications

Item		Description
Part number		FP2−Y64P
Insulation method		Optical coupler
Rated load voltage		5 to 24V DC
Load voltage range		4.75 to 26.4V DC
Maximum load current		0.1A (at 12 to 24V DC), 50mA (at 5V DC) (* Note)
Maximum surge current		0.3A
Off state leakage current		1μA or less
On state maximum voltage drop		1.5V or less (at 6 to 26.4V DC), 0.5V or less (at 6V DC or less)
Response time	**off → on**	0.1ms or less
	on → off	0.3ms or less
Internal current consumption (at 5V DC)		210mA or less
Power supply for driving internal circuit	**Voltage**	4.75 to 26.4V DC
	Current	270mA or less (at 24V DC)
Surge absorber		Zener diode
Fuse ratings		None
Common method (Output points per common)		32 points/common
Operating indicator		32-dot LED display (lit when on, switching)
External connection method		Connectors (MIL type two 40-pin)
Weight		Approx. 120g

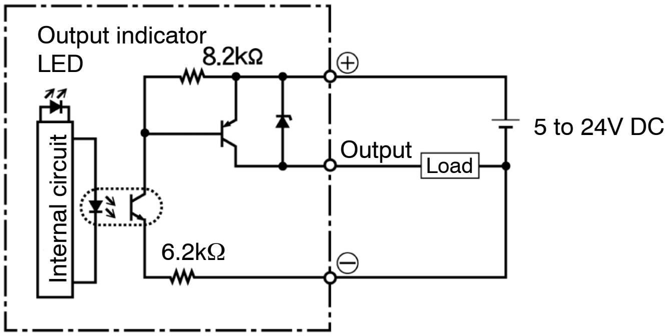
☞ **Note**

The load current will vary depending on the power supply for driving the internal circuit and the ambient temperature. Adjust the load current referring to the following range.

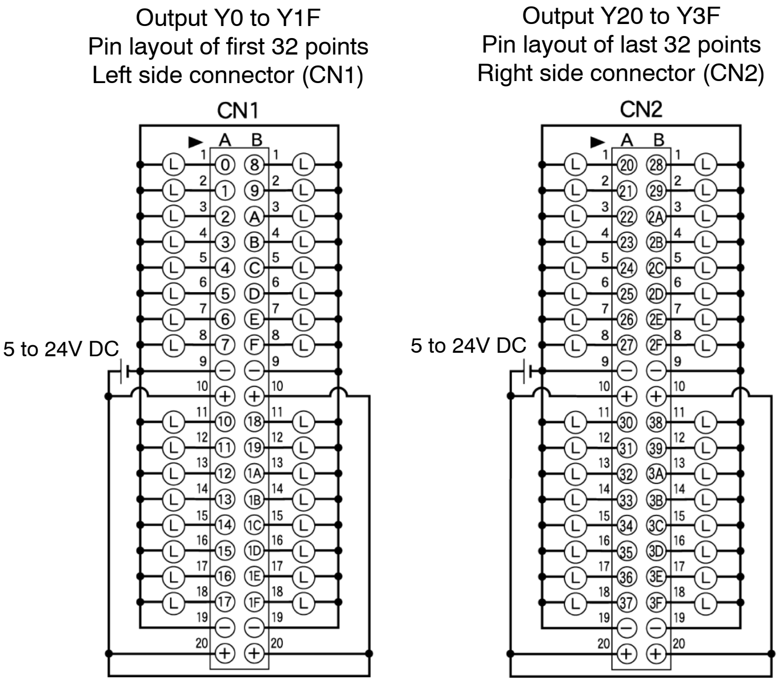




Internal Circuit Diagram



Pin Layout



Although ⊕ and ⊖ terminals are connected internally with the same connector. It is recommended that they also be connected externally.

For more information regarding the applicable connectors and terminals, refer to section 4.4.1.

2.11 I/O Mixed Units Specifications

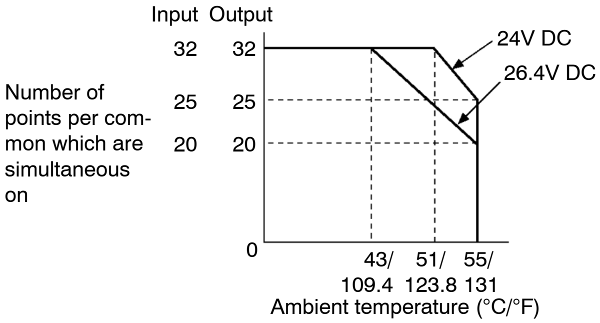
2.11.1 32–point Type DC Input/32–point Type Transistor (NPN) Output Unit

Specifications

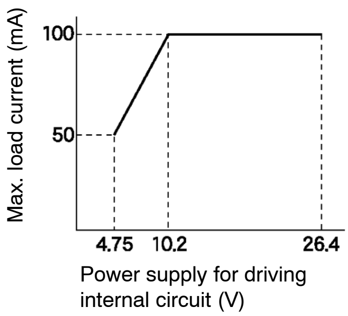
Item			Description
Part number			FP2–XY64D2T
Input specifications	Insulation method		Optical coupler
	Rated input voltage		24V DC
	Rated input current		Approx. 4.3mA (at 24V DC)
	Input impedance		Approx. 5.6kΩ
	Input voltage range		20.4 to 26.4V DC
	Min. on voltage/Min. on current		19.2V/4mA
	Max. off voltage/Max. off current		5.0V/1.5mA
	Response time	off → on	0.2ms or less
		on → off	0.3ms or less
	Common method (Input points per common)		32 points/common Either the positive or negative of the input power supply can be connected to common terminal.
Output specifications	Insulation method		Optical coupler
	Rated load voltage		5 to 24V DC
	Load voltage range		4.75 to 26.4V DC
	Maximum load current		0.1A (at 12 to 24V DC), 50mA (at 5V DC) (* Note)
	Maximum surge current		0.3A
	Off state leakage current		1μA or less
	On state maximum voltage drop		1V or less (at 6 to 26.4V DC), 0.5V or less (at 6V DC or less)
	Response time	off → on	0.1ms or less
		on → off	0.3ms or less
	Power supply for driving internal circuit	Voltage	4.75 to 26.4V DC
		Current	120mA or less (at 24V DC)
	Surge absorber		Zener diode
	Fuse ratings		None
	Common method (Output points per common)		32 points/common
Common specifications	Internal current consumption (at 5V DC)		150mA or less
	Operating indicator		32-dot LED display (lit when on, switching)
	External connection method		Connector (two 40-pin)
	Weight		Approx. 120g

Notes

- **Keep the number of input and output points per common which are simultaneously on within the following range as determined by the input voltage and ambient temperature.**

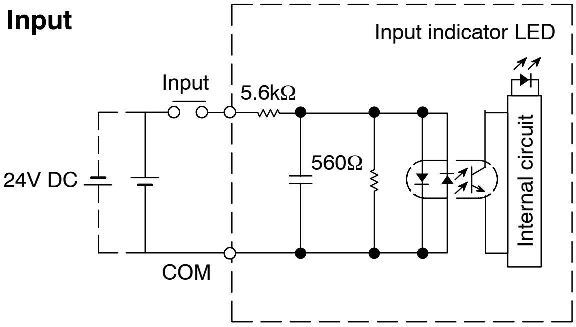


- **The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.**

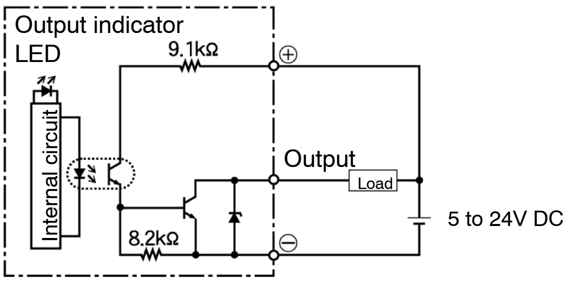


Internal Circuit Diagram

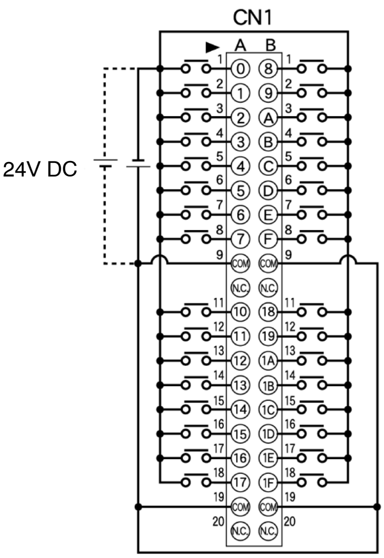
Input



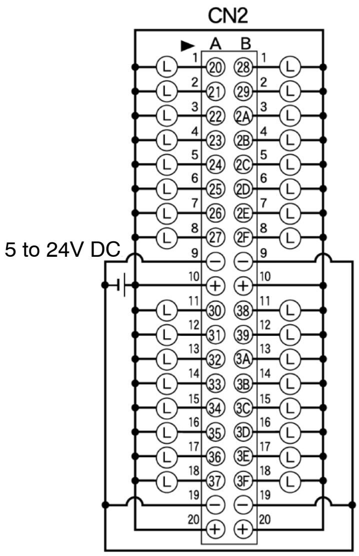
Output



Pin Layout



The COM pins of each connector are connected internally.



Although "+" and "–" terminals are connected internally with the same connector. It is recommended that they also be connected externally.

2.11.2 32–point Type DC Input/32–point Type Transistor (PNP) Output Unit

Specifications

Item			Description
Part number			FP2–XY64D2P
Input specifications	**Insulation method**		Optical coupler
	Rated input voltage		24V DC
	Rated input current		Approx. 4.3mA (at 24V DC)
	Input impedance		Approx. 5.6kΩ
	Input voltage range		20.4 to 26.4V DC
	Min. on voltage/ Min. on current		19.2V/4mA
	Max. off voltage/ Max. off current		5.0V/1.5mA
	Response time	**off → on**	0.2ms or less
		on → off	0.3ms or less
	Common method (Input points per common)		32 points/common Either the positive or negative of the input power supply can be connected to common terminal.
Output specifications	**Insulation method**		Optical coupler
	Rated load voltage		5 to 24V DC
	Load voltage range		4.75 to 26.4V DC
	Maximum load current		0.1A (at 12 to 24V DC), 50mA (at 5V DC) (* Note)
	Maximum surge current		0.3A
	Off state leakage current		1µA or less
	On state maximum voltage drop		1.5V or less (at 6 to 26.4V DC), 0.5V or less (at 6V DC or less)
	Response time	**off → on**	0.1ms or less
		on → off	0.3ms or less
	Power supply for driving internal circuit	**Voltage**	4.75 to 26.4V DC
		Current	130mA or less (at 24V DC)
	Surge absorber		Zener diode
	Fuse ratings		None
	Common method (Output points per common)		32 points/common
Common specifications	**Internal current consumption (at 5V DC)**		150mA or less
	Operating indicator		32-dot LED display (lit when on, switching)
	External Connection method		Connector (two 40-pin)
	Weight		Approx. 120g

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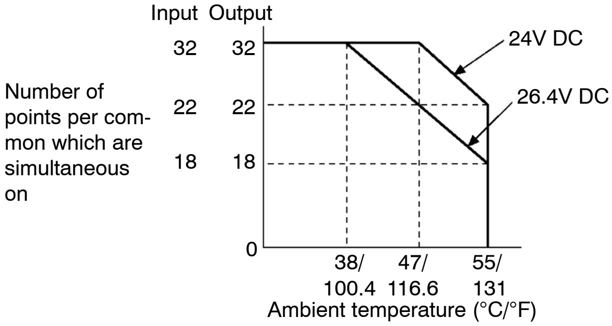
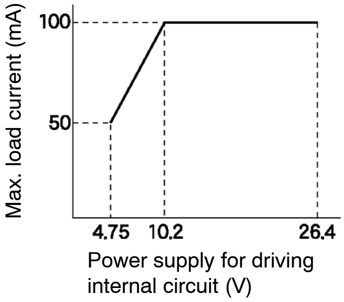
Notes

- **Keep the number of input and output points per common which are simultaneously on within the following range as determined by the input voltage and ambient temperature.**

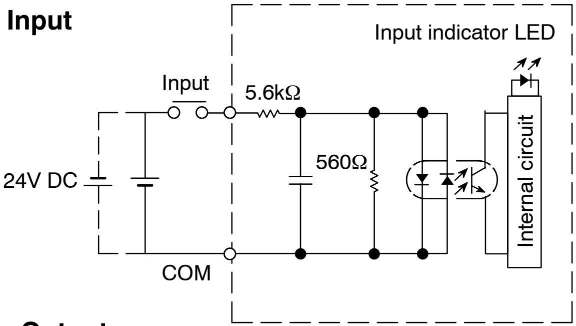


- **The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.**

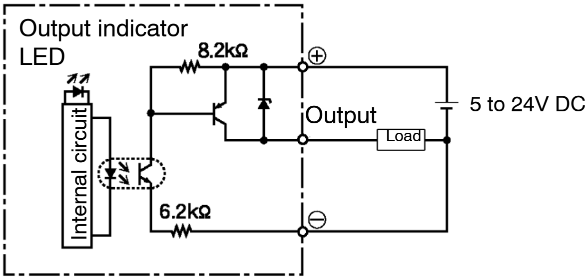


Internal Circuit Diagram

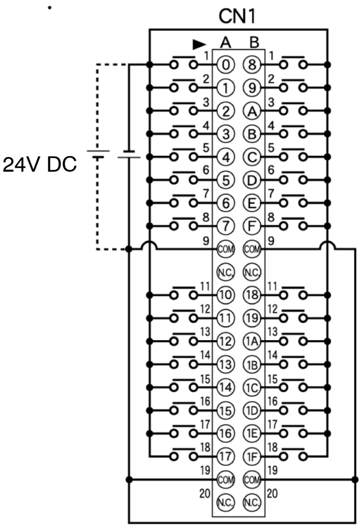
Input

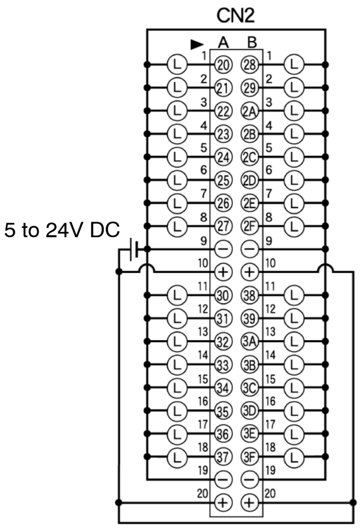


Output



Pin Layout





The COM pins of each connector are connected internally.

Although “+” and “–” terminals are connected internally with the same connector. It is recommended that they also be connected externally.

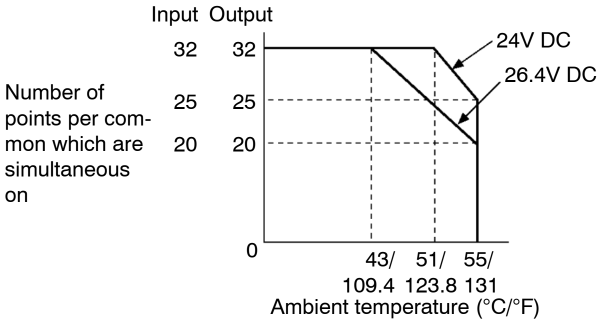
2.11.3 32–point Type DC Input with On Pulse Catch Input Function/ 32–point Type Transistor Output (NPN) Unit

Specifications

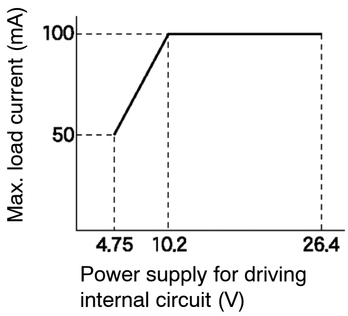
Item			Description
Part number			FP2–XY64D7T
Input specifications	**Insulation method**		Optical coupler
	Rated input voltage		24V DC
	Rated input current		Approx. 4.3mA (at 24V DC)
	Input impedance		Approx. 5.6kΩ
	Input voltage range		20.4 to 26.4V DC
	Min. on voltage/ Min. on current		19.2V/4mA
	Max. off voltage/ Max. off current		5.0V/1.5mA
	Response time	**off → on**	0.2ms or less (for X0 to X1F)
		on → off	0.3ms or less (for X0 to X1B) 1.0 to 5.0ms (X1C to X1F)
	Common method (Input points per common)		32 points/common Either the positive or negative of the input power supply can be connected to common terminal.
Output specifications	**Insulation method**		Optical coupler
	Rated load voltage		5 to 24V DC
	Load voltage range		4.75 to 26.4V DC
	Maximum load current		0.1A (at 12 to 24V DC), 50mA (at 5V DC)(* Note)
	Maximum surge current		0.3A
	Off state leakage current		1μA or less
	On state maximum voltage drop		1V or less (at 6 to 26.4V DC), 0.5V or less (at 6V DC or less)
	Response time	**off → on**	0.1ms or less
		on → off	0.3ms or less
	Power supply for driving internal circuit	**Voltage**	4.75 to 26.4V DC
		Current	120mA or less (at 24V DC)
	Surge absorber		Zener diode
	Fuse ratings		None
	Common method (Output points per common)		32 points/common
Common specifications	**Internal current consumption (at 5V DC)**		150mA or less
	Operating indicator		32-dot LED display (lit when on, switching)
	External connection method		Connector (two 40-pin)
	Weight		Approx. 120g

Notes

- **With a periodical interrupt function (1 ms), it is possible to read an on pulse input signal with a minimum pulse width of 0.4 ms. For detailed information about the on pulse catch input function ☛ section 2.11.5**
- **Keep the number of input and output points per common which are simultaneously on within the following range as determined by the input voltage and ambient temperature.**

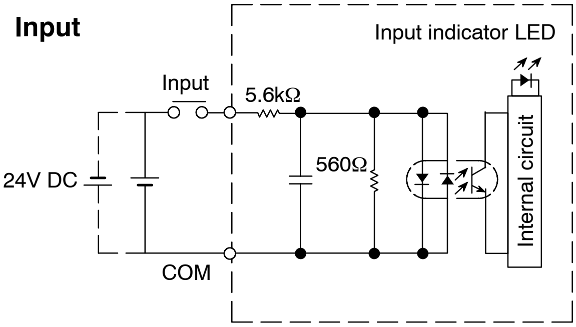


- **The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.**

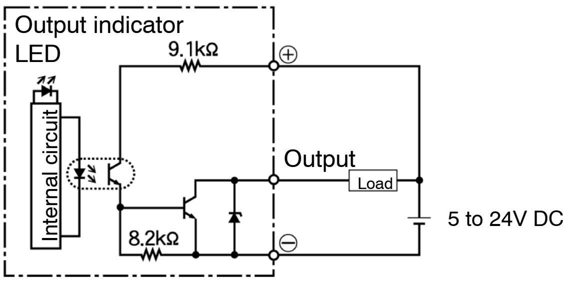


Internal Circuit Diagram

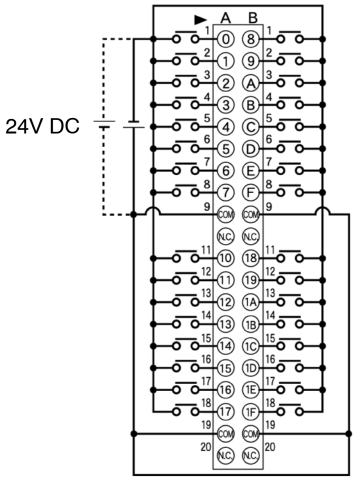
Input



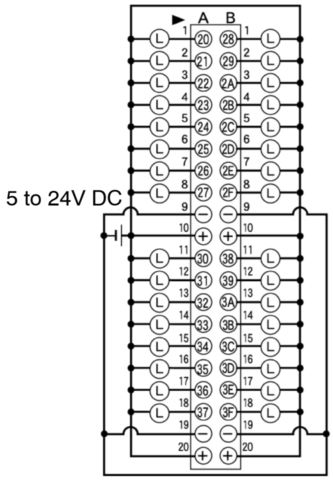
Output



Pin Layout



The COM pins of each connector are connected internally.



Although "+" and "−" terminals are connected internally with the same connector. It is recommended that they also be connected externally.

2.11.4 32–point Type DC Input with On Pulse Catch Input Function/ 32–point Type Transistor Output (PNP) Unit

Specifications

Item			Description
Part number			FP2–XY64D7P
Input specifications	Insulation method		Optical coupler
	Rated input voltage		24V DC
	Rated input current		Approx. 4.3mA (at 24V DC)
	Input impedance		Approx. 5.6kΩ
	Input voltage range		20.4 to 26.4V DC
	Min. on voltage/ Min. on current		19.2V/4mA
	Max. off voltage/ Max. off current		5.0V/1.5mA
	Response time	off → on	0.2ms or less (for X0 to X1F)
		on → off	0.3ms or less (for X0 to X1B) 1.0 to 5.0ms (for X1C to X1F)
	Common method (Input points per common)		32 points/common Either the positive or negative of the input power supply can be connected to common terminal.
Output specifications	Insulation method		Optical coupler
	Rated load voltage		5 to 24V DC
	Load voltage range		4.75 to 26.4V DC
	Maximum load current		0.1A (at 12 to 24V DC), 50mA (at 5V DC)(* Note)
	Maximum surge current		0.3A
	Off state leakage current		1μA or less
	On state maximum voltage drop		1.5V or less (at 6 to 26.4V DC) 0.5V or less (at 6V DC or less)
	Response time	off → on	0.1ms or less
		on → off	0.3ms or less
	Power supply for driving internal circuit	Voltage	4.75 to 26.4V DC
		Current	130mA or less (at 24V DC)
	Surge absorber		Zener diode
	Fuse ratings		None
	Common method (Output points per common)		32 points/common
Common specifications	Internal current consumption (at 5V DC)		150mA or less
	Operating indicator		32-dot LED display (lit when on, switching)
	External connection method		Connector (two 40-pin)
	Weight		Approx. 120g

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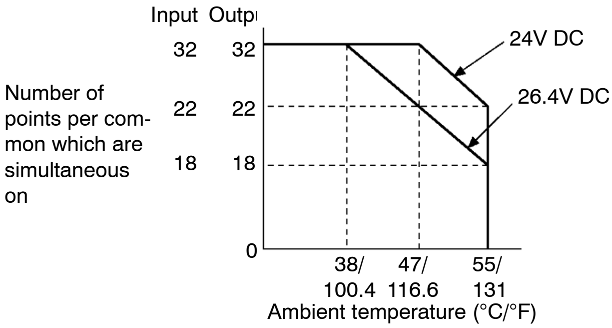
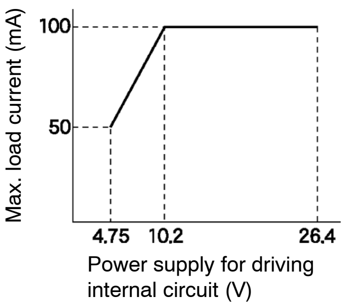
Notes

- **With a periodical interrupt function (1ms), it is possible to read an on pulse input signal with a minimum pulse width of 0.4ms. For detailed information about the on pulse catch input function ☛ section 2.11.5**
- **Keep the number of input and output points per common which are simultaneously on within the following range as determined by the input voltage and ambient temperature.**

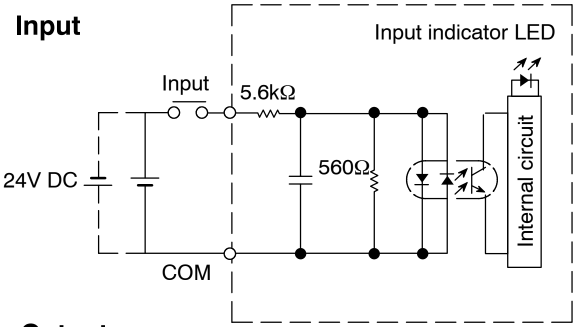


- **The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.**

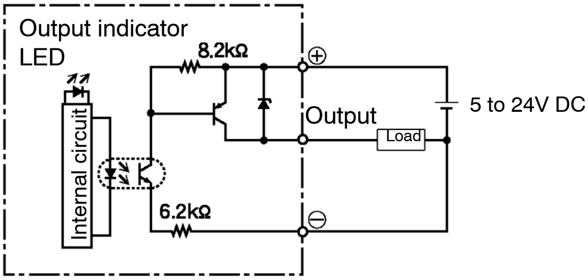


Internal Circuit Diagram

Input

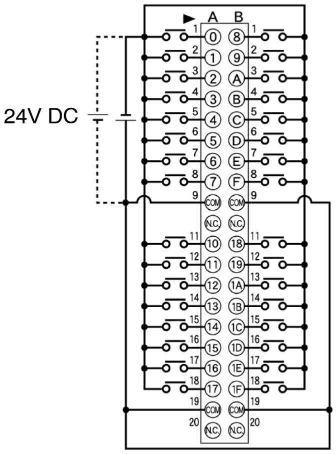


Output

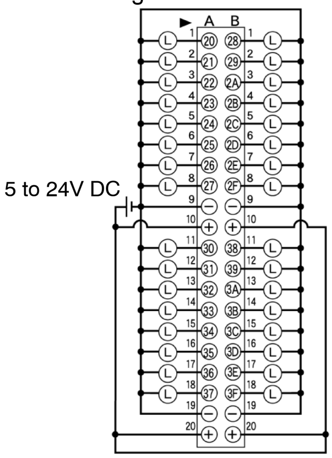


Pin Layout

Input X0 to X1F
Pin layout of first 32 points
Left side connector



Output Y20 to Y3F
Pin layout of last 32 points
Right side connector



The COM pins of each connector are connected internally.

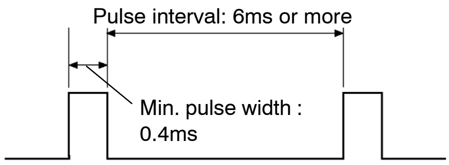
Although “+” and “–” terminals are connected internally with the same connector. It is recommended that they also be connected externally.

2.11.5 On Pulse Catch Input Function

The I/O mixed unit (FP2–XY64D7T/FP2–XY64D7P) is equipped with “On pulse catch input” function. The on pulse catch input function has a delay circuit built into the input and is used in combination with a periodical interrupt function to make possible the reading of on pulses with extremely small widths.

Readable pulse signals

Minimum pulse width: 0.4ms
Pulse interval: 6ms or more



Method

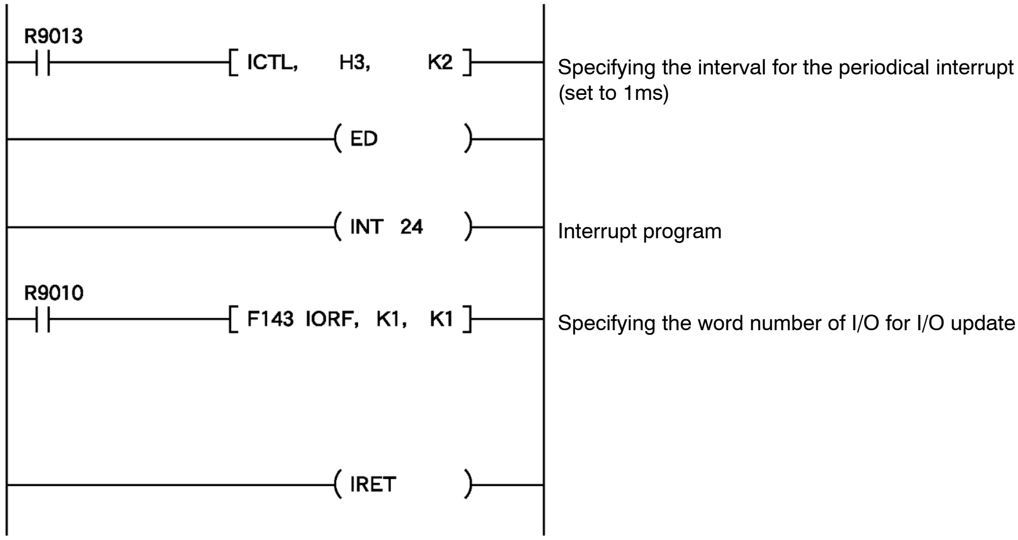
In the program, specify the interval of periodical interrupt and the word number of I/O.

Considerations

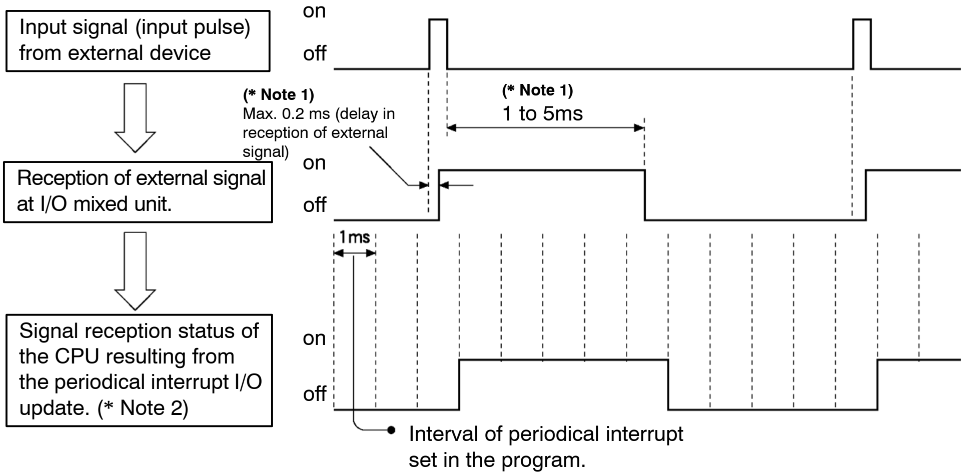
The interval for the periodical interrupt is determined by the interrupt control instruction. Specify the pulse catch I/O (input) with the **ICTL** and **F143 (IORF)** instructions.

Program example

When an I/O mixed unit with on pulse catch input function is installed to slot “0” of the backplane.



Operation of pulse catch



Notes

1) **Reception of external signal at the I/O mixed unit.**
   Within 0.2ms of the leading edge of the external signal, the I/O mixed unit will go on. This on status will be held for 1 to 5ms (the length of time the status is held will depend on the unit).

2) **Reception of input at CPU that is executing a periodical interrupt.**
   The signal from the I/O mixed unit is read by the periodical interrupt.

Chapter 3

I/O Allocation

3.1 Fundamentals of I/O Allocation

3.1.1 I/O Allocation and Registering

I/O allocation is the process of assigning an I/O number to each unit. Registering refers to registering the I/O allocations in the system register of the CPU.

3.1.1.1 Types of I/O Allocation Methods

There are 3 types of allocation methods: I/O mount allocation, arbitrary allocation, and automatic allocation.

I/O mount allocation

Using the programming tool software (NPST-GR/FPWIN GR), the allocation condition of the mounted units is recorded, as is, to the system register of the CPU.

Arbitrary allocation

The programming tool software (NPST-GR/FPWIN GR) is used to create I/O allocations and register them in the system register of the CPU. In this case, no deviations in I/O numbers will occur if a unit mounting error was made.

Automatic allocation

If units are installed, allocation will take place when the power is turned on based on the states of the installed units.

☞ **Note**

Automatic allocation only assigns I/O numbers to mounted units. It does not register the allocations.

3.1.1.2 Precautions Regarding Registering of I/O Allocation

If registering is not performed when using arbitrary allocation:

Automatic allocation will be performed, and allocation will be based on the state of the installed units.

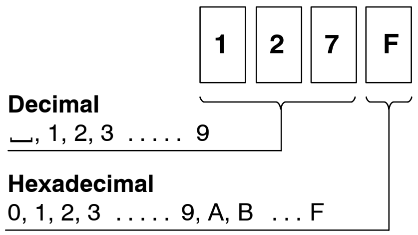
If I/O registration has already been performed:

If the registered information is different from the actual state of installation, such as when a unit is changed to a different type or the installation position is changed, normal operation will not take place. In this case, perform registration once again.

3.1.1.3 How to Count the I/O Numbers and Express the Occupied Points

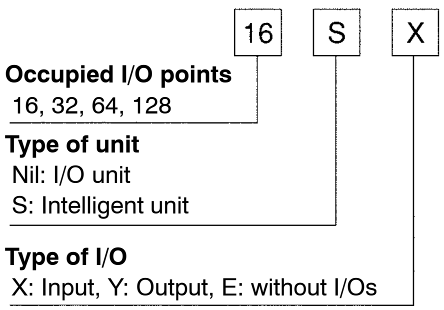
How to count the I/O numbers (relay numbers)

Since I/O number are handled in units of 16 points, they are expressed as a combination of decimal and hexadecimal numbers as shown below.



How to express the occupied points

In the programming tool and this manual, the occupied points are expressed in the following fashion for convenience.



3.1.2 Table of Occupied I/O Points by Unit

Name		Part number	Occupied I/O point	Number of occupied slot
CPU	**Standard type CPU**	FP2–C1	–	1
	CPU with 64 points input	FP2–C1D	64X	2
	CPU with S-LINK	FP2–C1SL	(* Note 1)	2 (* Note 2)
FP2SH CPU	**FP2–C2L**	AFP2221	–	1
	FP2–C2	AFP2231	–	1
	FP2–C2P	AFP2235	–	1
	FP2–C3P	AFP2255	–	1
Remote I/O Slave Unit		FP2–RMS	–	1
Input unit	**16-point type DC input**	FP2–X16D2	16X	1
	32-point type DC input	FP2–X32D2	32X	1
	64-point type DC input	FP2–X64D2	64X	1
Output unit	**16-point type relay output**	FP2–Y16R	16Y	1
	6-point type relay output	FP2–Y6R	16Y	1
	16-point type transistor (NPN) output	FP2–Y16T	16Y	1
	16-point type transistor (PNP) output	FP2–Y16P	16Y	1
	32-point type transistor (NPN) output	FP2–Y32T	32Y	1
	32-point type transistor (PNP) output	FP2–Y32P	32Y	1
	64-point type transistor (NPN) output	FP2–Y64T	64Y	1
	64-point type transistor (PNP) output	FP2–Y64P	64Y	1
I/O mixed unit	**32-point type DC input/32-point type transistor (NPN) output**	FP2–XY64D2T FP2–XY64D7T	32X, 32Y	1
	32-point type DC input/32-point type transistor (PNP) output	FP2–XY64D2P FP2–XY64D7P	32X, 32Y	1

☛ next page

3.1 Fundamentals of I/O Allocation

Name		Part number		Occupied I/O point	Number of occupied slot
Intelligent unit	Analog input unit	FP2−AD8VI, FP2−AD8X, FP2−RTD		128SX	1
	Analog output unit	FP2−DA4		64SY	1
	High−speed counter unit	FP2−HSCT		32SX, 32SY	1
		FP2−HSCP			
	Pulse I/O unit	FP2−PXYT		32SX, 32SY	1
		FP2−PXYP			
	Positioning unit (2-axis type)	FP2−PP2		32SX, 32SY	1
	Positioning unit (4-axis type)	FP2−PP4		64SX, 64SY	1
	Positioning unit (Multifunction type) 2−axis type	Transistor output type	FP2−PP21	32SX, 32SY	1
		Line driver output type	FP2−PP22		
	Positioning unit (Multifunction type) 4−axis type	Transistor output type	FP2−PP41	64SX, 64SY	1
		Line driver output type	FP2−PP42		
	Positioning unit RTEX (2-axis type)	FP2−PN2AN		128SX, 128SY	1
	Positioning unit RTEX (4-axis type)	FP2−PN4AN			
	Positioning unit RTEX (8-axis type)	FP2−PN8AN			
	Positioning Unit (Interpolation type) 2−axis type	Transistor output type	FP2−PP2T	32SX, 32SY	1
		Line driver output type	FP2−PP2L		
	Positioning Unit (Interpolation type) 4−axis type	Transistor output type	FP2−PP4T	64SX, 64SY	1
		Line driver output type	FP2−PP4L		
	Multi communication unit	FP2−MCU		16SX, 16SY	1
	Serial data unit	FP2−SDU		16SX, 16SY	1
	C.C.U.	FP2−CCU		16SE (0SE) (* Note 3)	1
	S-LINK unit	FP2−SL2		(* Note 1)	1
	Multi-wire link unit	FP2−MW		16SE (0SE) (* Note 3)	1
	ET−LAN unit	FP2−ET1		32SX, 32SY (0SE)	1
	MEWNET−VE Link unit	FP2−VE		32SX, 32SY (0SE)	1
	FNS Unit	FP2−FNS		16SE (0SE) (* Note 3)	1
	FMU Unit	PROFIBUS	FP2−DPV1−M	16SE (0SE) (* Note 3)	1
		Device Net	FP2−DEV−M		
		CAN open	FP2−CAN−M		

Notes

1) The “occupied I/O point” of S-LINK unit and CPU with S-LINK, will vary depending on the unit settings. For details, refer to “FP2 S-LINK Manual”.
2) When using a CPU with S-LINK, the functionality of the slots are increased, and slot numbers can be allocated as if two S-LINK units were installed. For more details, refer to “FP2 S-LINK Manual”.
3) The occupied point can be set to “0” with arbitrary allocation.
4) When the handshake by I/O is not used, the number of occupied points can be set to “0” by allocating arbitrarily.

3.2 Arbitrary Allocation

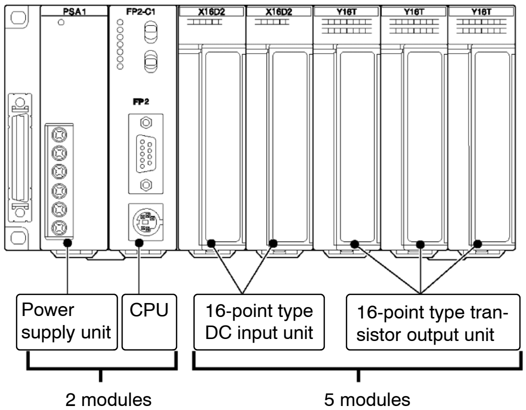
3.2.1 Using Arbitrary Allocation

In the case of arbitrary allocation, I/O allocations are decided at the time of system design, and the allocations are registered in the PLC using a programming tool such as NPST-GR/FPWIN GR software.

At this time, registration can be performed even if the I/O units are not yet installed on the backplane according to the allocations. However, before operation the I/O units must be installed and set as required by the system design.

3.2.2 Allocation Example of CPU Backplane

Backplane: 7-module type
Power supply unit: 1 module
CPU: 1 module
I/O units used:
16-point type DC input unit: 2 units
16-point type transistor output unit: 3 units



Registering with programming tool software

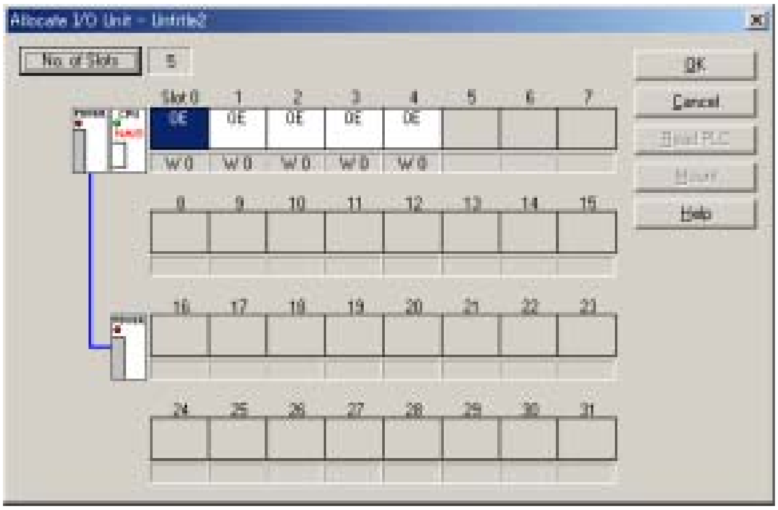
Preparations

Display the allocation screen.

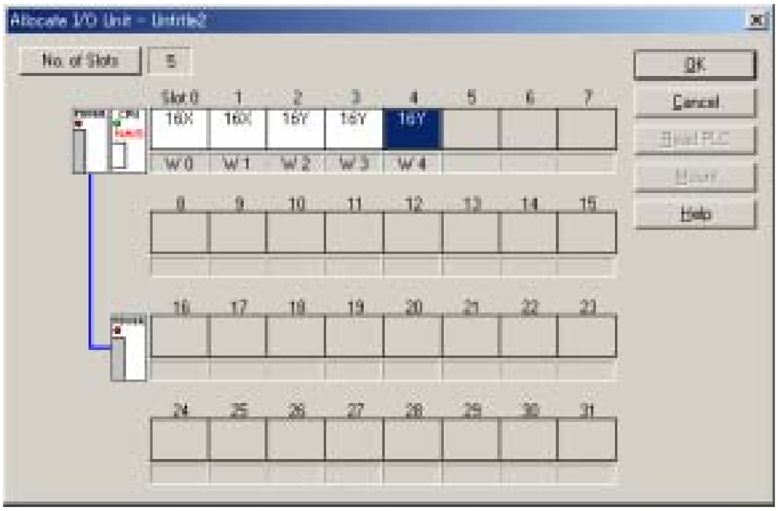
1. **Set the “FPWIN GR” software to OFFLINE mode.**
2. **On the “Option” menu, select “Allocate I/O Map”.**

Creating allocations

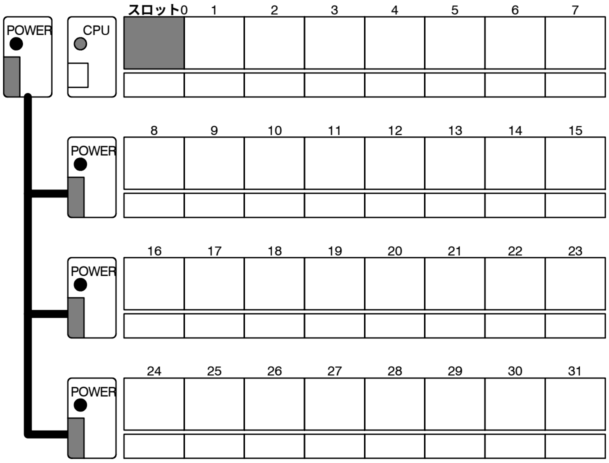
1. **In “No. of Slots”, enter the number of modules(number of slots) to used. OE is assigned to the slots after they are specified.**
   In this case, the number of modules that can be used is 5, so enter “5”.



2. **Assign input (X) or output (Y) according to the I/O units to be installed in each slot.**
   Assign 16X to slots 0 and 1, and 16Y to slots 2 through 4.



When a system is configured with the FP2 backplane H type (AFP25***H), the display is shown as AFP25*** since no exclusive tool display is not available for the H type. The actual system is as shown below. (No indication of the power supply unit and expansion unit.)



Registering contents of allocation

Write the contents of allocation to the System register of the CPU.

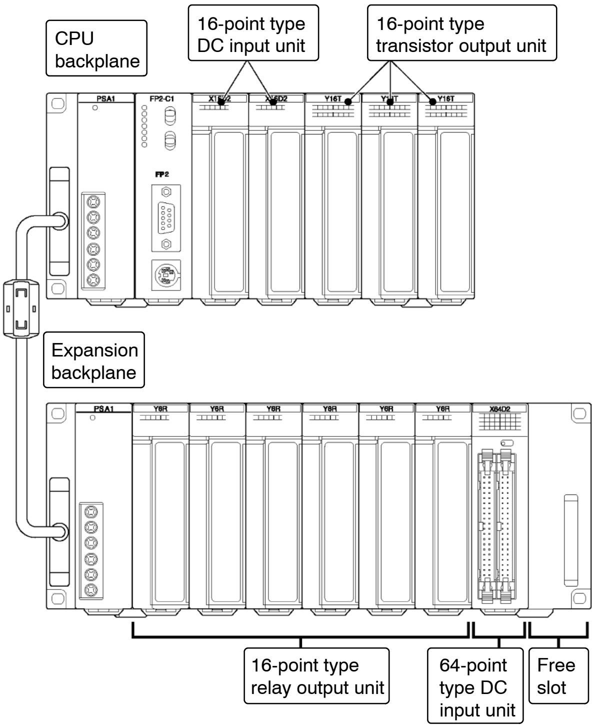
1. **On the “Online” menu, select “Online Edit Mode”.**
2. **On the “File” menu, select “Download to PLC”.**
   The program is transferred to the PLC (programmable controller), and the contents of allocation are simultaneously written to the PLC as part of its system register settings.

3.2.3 Allocation Example of Expansion Backplane

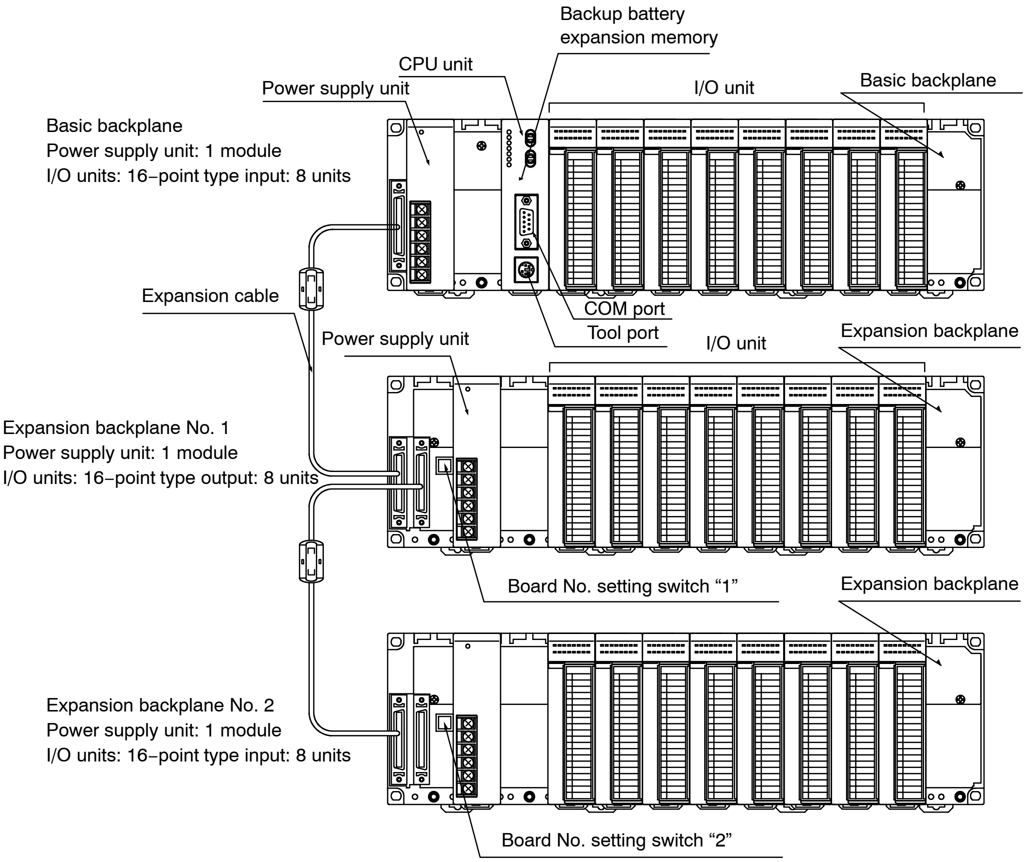
3.2.3.1 When Using FP2 Backplane

CPU backplane
Backplane: 7-module type
Power supply unit: 1 module
CPU: 1 module
I/O units:
16-point type DC input unit: 2 units
16-point type transistor output unit: 3 units

Expansion backplane
Backplane: 9-module type
Power supply unit: 1 module
I/O units:
16-point type relay output unit: 6 units
64-point type DC input unit: 1 unit

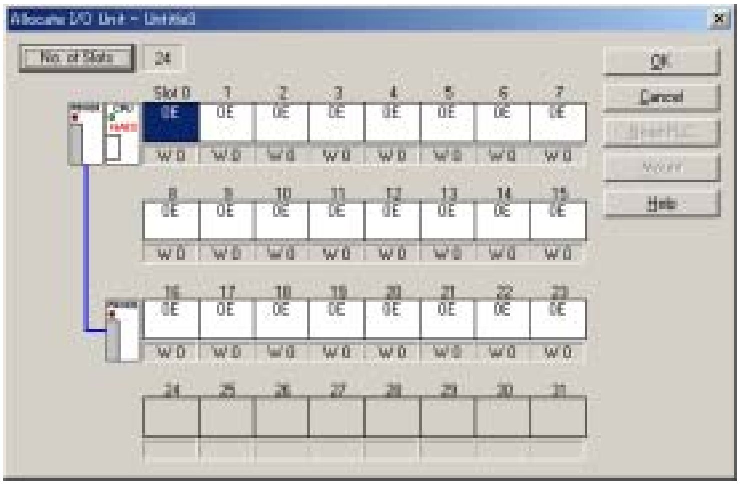


3.2.3.2 When Using FP2 Backplane H Type

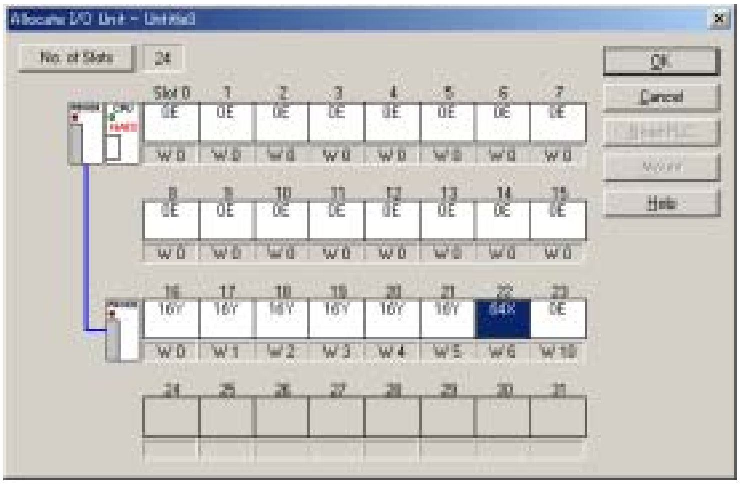


Registering with programming tool software (FPWIN GR)
Create allocations

1. **In “No. of Slots”, add 16 to the number of modules used on the expansion backplane and enter the result.**
   OE is assigned to each of the specified slots. In this case, enter “24”.



2. **Assign input (X) or output (Y) according to the I/O units to be installed in each slot.**
   In the example, assign 16X to slots 0 through 7, 16Y to slots 8 through 15, and 16X to slots 16 through 23.



Registering contents of allocation

Write the contents of allocation to the system register of the CPU.

1. **On the “Online” menu, select “Online Edit Mode”.**
2. **On the “File” menu, select “Download to PLC”.**
   The program is transferred to the PLC (programmable controller), and the contents of allocation are simultaneously written to the PLC as part of its system register settings.

3.3 I/O Mount Allocation

3.3.1 Using I/O Mount Allocation

The I/O allocation state of mounted units is directly registered.

If an expansion backplane has been added on the FP2 backplane, the number of slots for I/O units on the CPU backplane is taken as 16 slots. (The FP2 backplane H type occupies 8 slots only.)

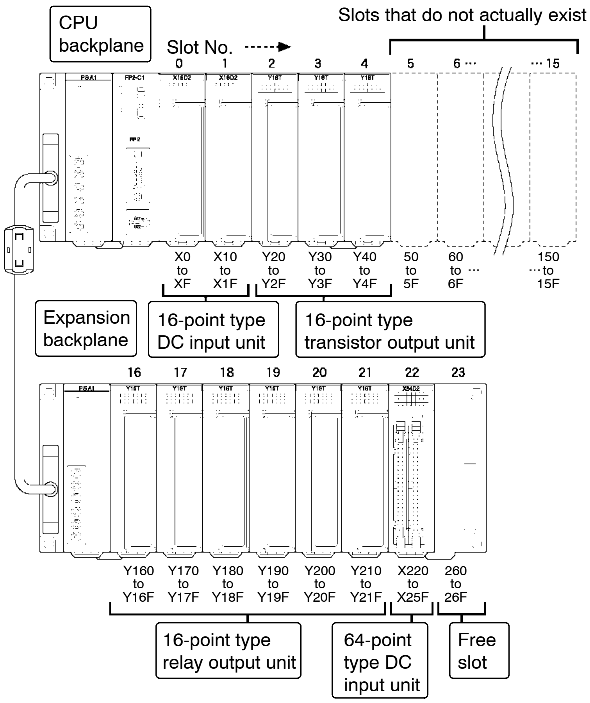
For a slot with no unit mounted, an equivalent of 16 points (16E) is allocated.

3.3.1.1 Example of I/O Mount Allocation

The I/O number in the diagram is the result of execution of I/O mount allocation.

CPU backplane
Backplane: 7-module type
Power supply unit: 1 module
CPU: 1 module
I/O units:
16-point type DC input unit: 2 units
16-point type transistor output unit: 3 units

Expansion backplane
Backplane: 9-module type
Power supply unit: 1 module
I/O units :
16-point type relay output unit: 6 units
64-point type DC input unit: 1 unit



At the expansion backplane, I/O numbers are allocated continuing from the last number allocated to slots that do not actually exist on the CPU backplane.

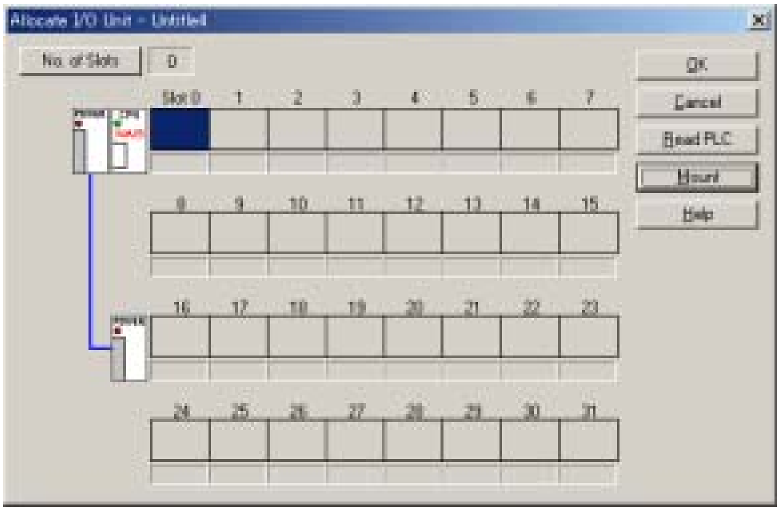
3.3.1.2 Procedure for I/O Mount Allocation

Preparations

Turn on the power of the PLC and set the mode selector of the CPU to PROG. mode. Set the programming tool software to online monitor.

Procedure:

1. **On the “Option” menu, select “Allocate I/O Map”.**



2. **Click [Mount] button.**
   The following message appears, and then select [Yes].

The appearance of the allocation of the mounted units will be read into and displayed on the FPWIN GR screen. At the same time, the contents of allocation will be registered in the system registers of CPU.

3.4 Automatic Allocation

3.4.1 Using Automatic Allocation

After turning on the power, I/O numbers are determined by the I/O unit installation positions and assigned in order beginning from the left side of the CPU backplane.

If an expansion backplane has been added on the FP2 backplane, the number of slots for I/O units on the CPU backplane is taken as 16 slots. (The FP2 backplane H type occupies 8 slots only.)

For a slot with no unit mounted, an equivalent of 16 points (16E) is allocated.

In the case of automatic allocation, I/O numbers are assigned based on the installed I/O units each time the power is turned on.

Note

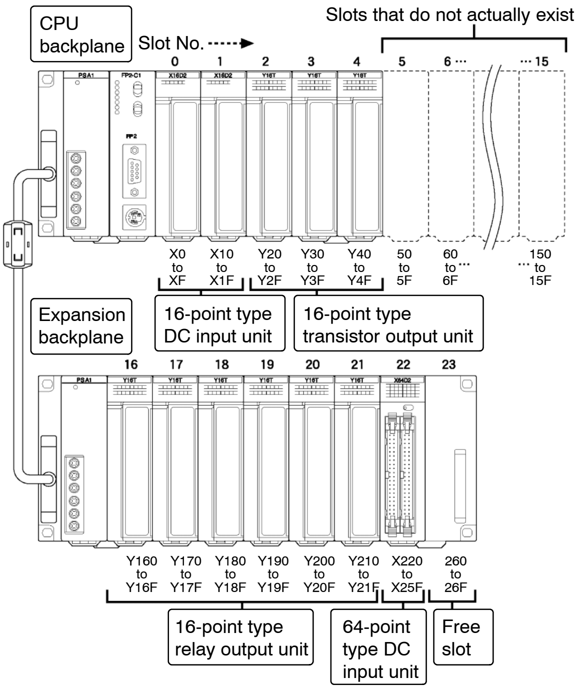
With automatic allocation, the contents of allocation are not registered to the system register.

3.4.1.1 Example of Automatic Allocation

The I/O numbers in the illustration are the allocated I/O numbers using automatic allocation.

CPU backplane
Backplane: 7-module type
Power supply unit: 1 module
CPU: 1 module
I/O units:
16-point type DC input unit: 2 units
16-point type transistor output unit: 3 units

Expansion backplane
Backplane: 9-module type
Power supply unit: 1 module
I/O units:
16-point type relay output unit: 6 units
64-point type DC input unit: 1 unit



At the expansion backplane, I/O numbers are allocated continuing from the last number allocated to slots that do not actually exist on the CPU backplane.

3.4.1.2 Procedure for Automatic Allocation

Automatic allocation is executed when the power is turned on.
If I/O allocations have previously been registered using arbitrary allocation or I/O mount allocation, automatic allocation is not executed.

Clear the registered allocations and then turn on the power once again (☛ section 3.5).

The result of the automatic allocation will be the same as for I/O mount allocation.

3.5 Procedure for Clearing Registered Content

3.5.1 Meaning of Clearing Registered Content

To repeat the I/O allocation, it is necessary to clear registered content. Registered content is cleared by initializing the system registers.

Note

System registers not related to I/O allocations are also initialized. If you only want to change the registered I/O allocations, do not initialize the system registers. Instead, use arbitrary allocation (☛ section 3.2).

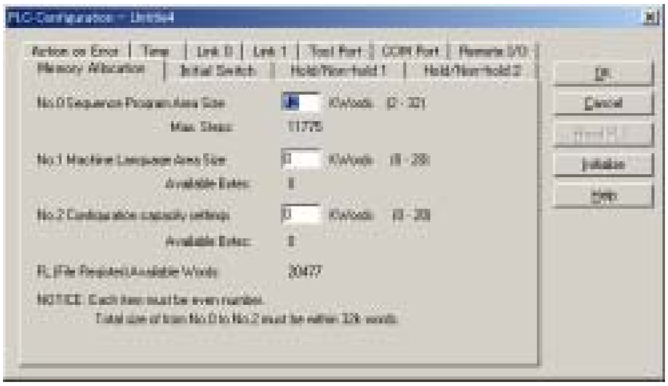
3.5.2 Clearing Content Using Programming Tool Software

Preparations

Set the “FPWIN GR” tool software to online monitor.

Procedure:

1. **On the “Option” menu, select “PLC Configuration”.**



2. **Click [Initialize] button.**

Select “PLC Configuration + I/O Unit + Remote I/O” and Click “OK” button. The content of system registers and I/O allocations will be cleared.

3.6 I/O Numbers of Free Slots

3.6.1 I/O Numbers of Free Slots

I/O numbers are also assigned to modules (slots) where no units are installed. Programming and system construction can be made more efficient by using an appropriate manner of assigning I/O numbers.

3.6.2 Differences Due to Allocation Methods

The manner of assigning I/O numbers differs depending on the I/O allocation method.

3.6.2.1 When Arbitrary Allocation is Used

I/O point numbers can assigned as desired.

Advantage

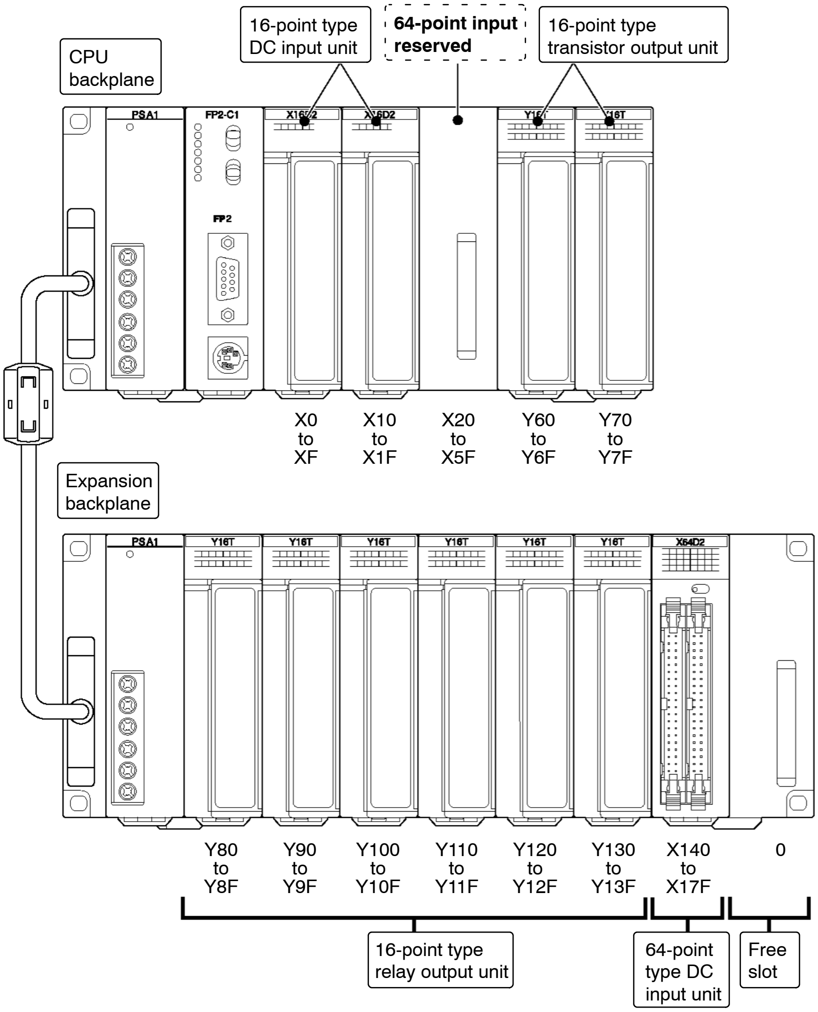
When designing a system with the intention of adding units in the future, you can use arbitrary allocation to assign ahead of time the I/O point numbers of the units to be added.

If no assignment is made, 0 is assigned.

By using I/O number assignments that take into account future expansion when creating the program, no discrepancies will occur when the new units are added on. Planning ahead for expansion improves efficiency.

☛ next page

Example of pre-assigning I/O numbers for a 64-point type input unit to a free slot

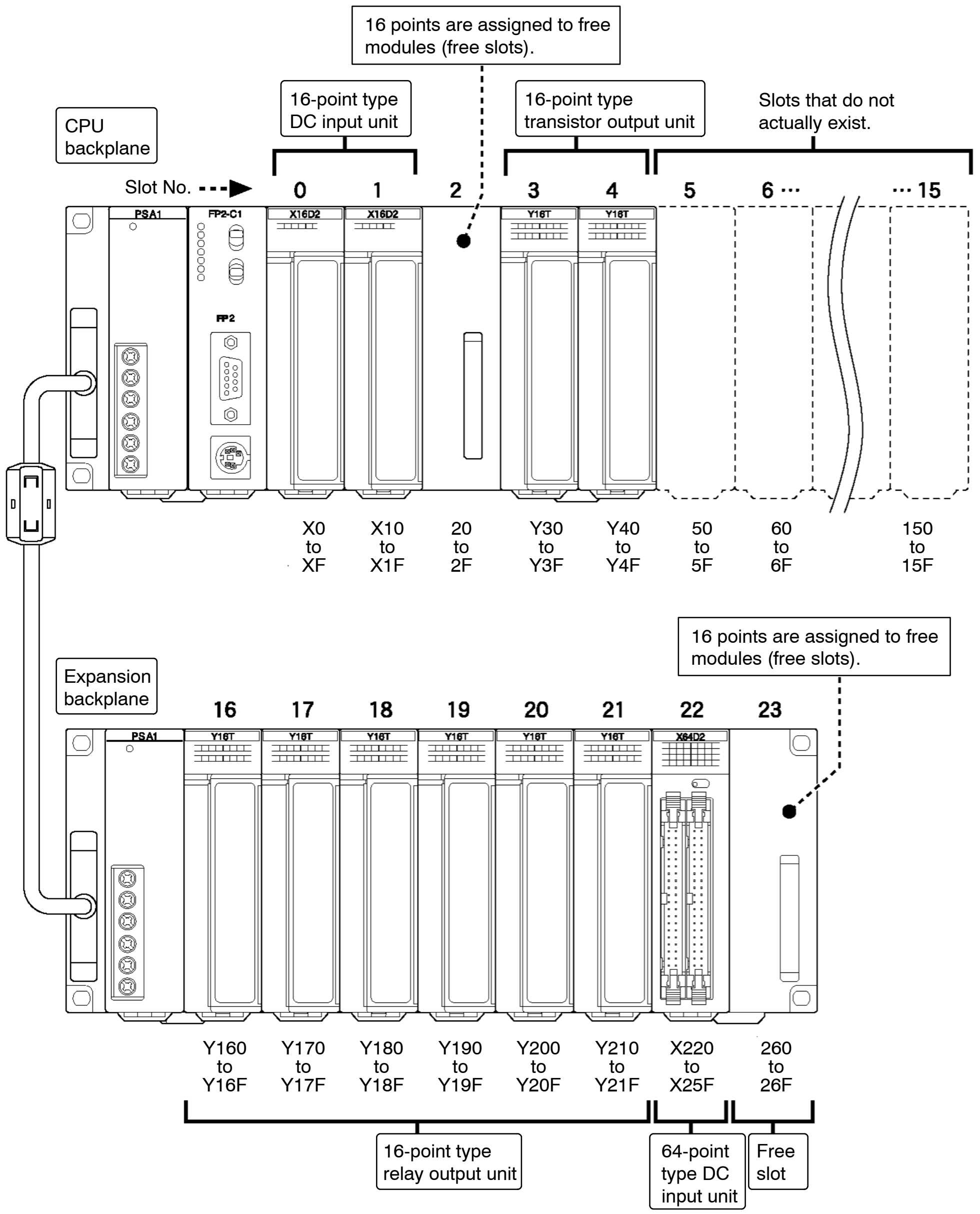


3.6.2.2 When I/O Mount Allocation is Used

When I/O mount allocation is executed, 16 points are uniformly assigned to each free slot.

Advantage

When the I/O unit that occupy 16 points is added, there is no need to worry about I/O number discrepancies.



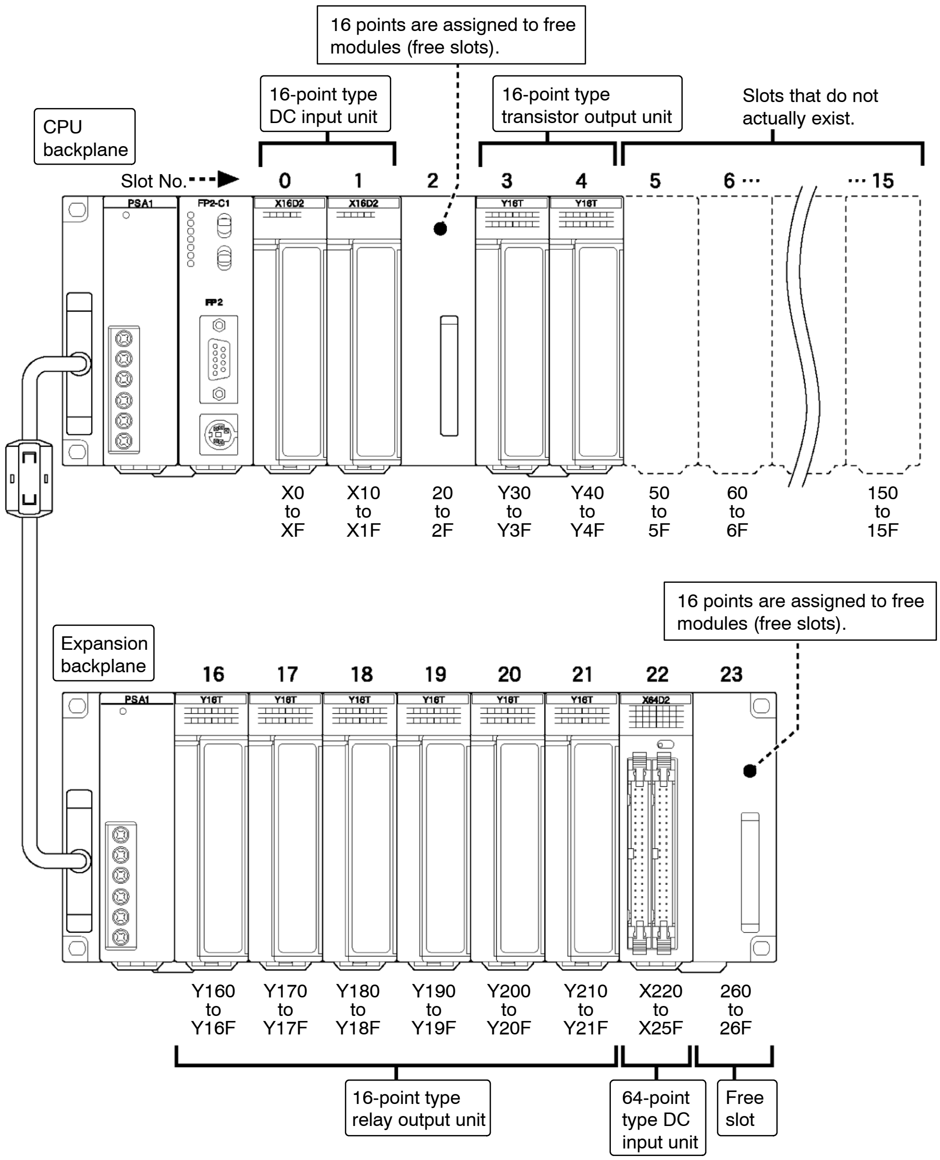
3.6.2.3 When Automatic Allocation is Used

When automatic allocation is executed, 16 points are uniformly assigned to each free slot.

With automatic allocation, the contents of allocation are not registered. Assignments are performed each time the power of PLC is turned on based on the units actually mounted.

Advantage

Automatic allocation is convenient when frequent structural changes are conducted such as during trial runs and testing of the program. It is convenient when using a large number of standard I/O units (units that occupy 16 points).



3.6 I/O Numbers of Free Slots

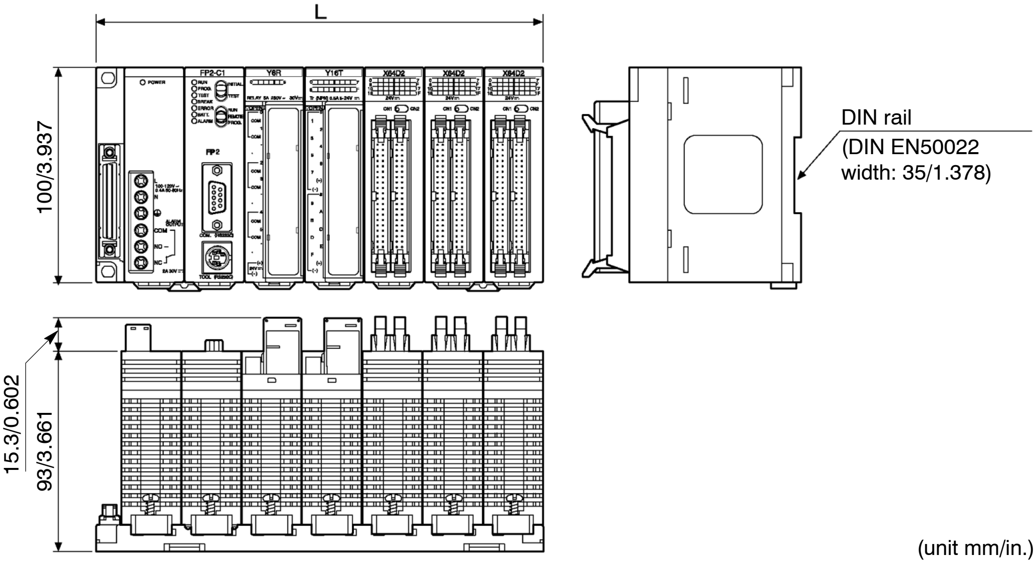
Chapter 4

Installation and Wiring

4.1 Installation

4.1.1 Installation Space and Environment

Dimensions



(unit mm/in.)

Type of FP2 backplane	Type of FP2 backplane H type	L (mm/in.)
5-module type	————	140/5.512
7-module type	————	209/8.228
9-module type	————	265/10.433
12-module type	**11−module type (Basic backplane)** **10−module type (Expansion backplane)**	349/13.740
14-module type	————	405/15.945

The 5-module type backplane has no connector for expansion.
Installation to a DIN rail is possible.

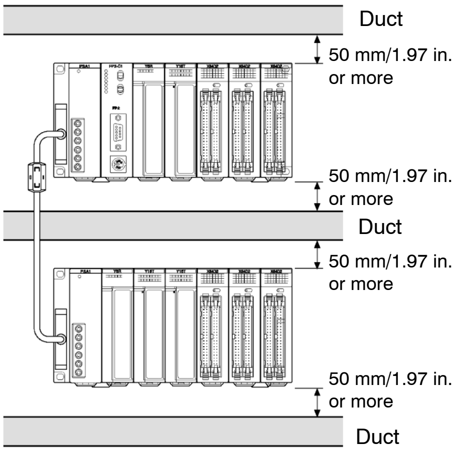
Installation location

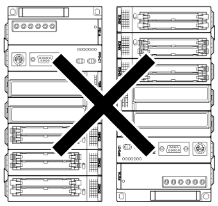
Be sure to maintain a sufficient distance from wiring ducts, and other machines below and above the unit for proper ventilation.

Do not install the units stacked up or horizontally. Doing so will prevent proper cooling of the unit and cause overheating inside the PLC (programmable controller).

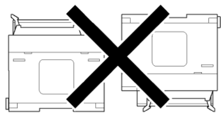
Do not install the unit above devices which generate heat such as heaters, transformers or large scale resistors.

In order to eliminate any effects from noise emission, power wires and electromagnetic devices should be kept at least 100 mm/13.937 in. away from the surfaces of the unit. When installing the unit behind the doors of the operation panel, be especially careful to maintain these distances.

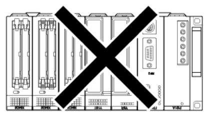




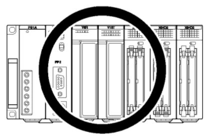
Incorrect: Stacked-up installation



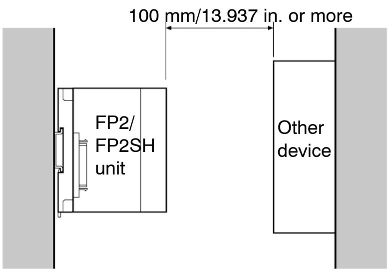
Incorrect: Horizontal installation



Incorrect: Upside-down installation

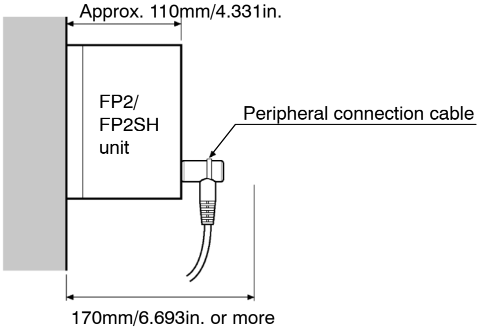


Correct: Proper installation



Space of Programming Tool Connection

Leave a space of at least 170mm/6.693in. from the mounting surface for programming tool connections and wiring.



Operating environment
(Use the unit within the range of the general specifications when installing)

Ambient temperatures:0 to +55 °C

Ambient humidity: 30% to 85% RH (at 25 °C, non−condensing)

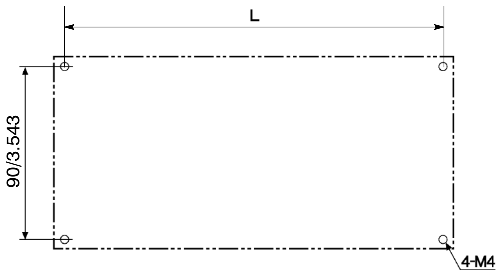
For use in pollution Degree 2 environment.

- Do not use it in the following environments.
- Direct sunlight
- Sudden temperature changes causing condensation.
- Inflammable or corrosive gas.
- Excessive airborne dust, metal particles or saline matter.
- Benzine, paint thinner, alcohol or other organic solvents or strong alkaline solutions such as ammonia or caustic soda.
- Direct vibration, shock or direct drop of water.
- Influence from power transmission lines, high voltage equipment, power cables, power equipment, radio transmitters,or any other equipment that would generate high switching surges. (100mm or more)

4.1.2 Mounting Method

4.1.2.1 Backplane

Mounting Hole Dimensions



(Unit mm/in.)

FP2 backplane

Type of backplane	Part number	L (mm/in.)
5-module type	FP2–BP05	130/5.118
7-module type	FP2–BP07	199/7.835
9-module type	FP2–BP09	255/10.039
12-module type	FP2–BP12	339/13.346
14-module type	FP2–BP14	395/15.551

FP2 backplane H type

Type of backplane	Part number	L (mm/in.)
11-module type (Basic backplane)	FP2–BP11MH	339/13.346
10-module type (Expansion backplane)	FP2–BP10EH	339/13.346

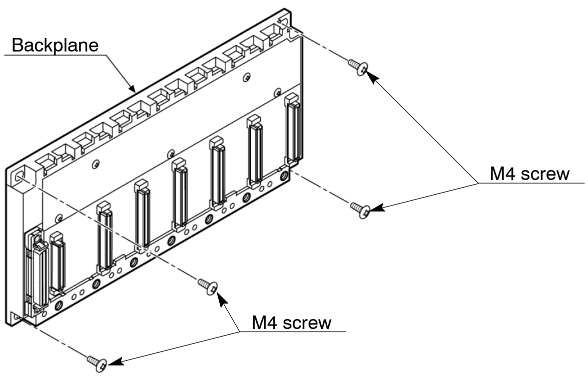
Attaching with Screws

☞ **Note**

Secure the backplane while the unit is not installed.
(Tightening torque: 0.9 to 1.1 N·m)

Procedure:

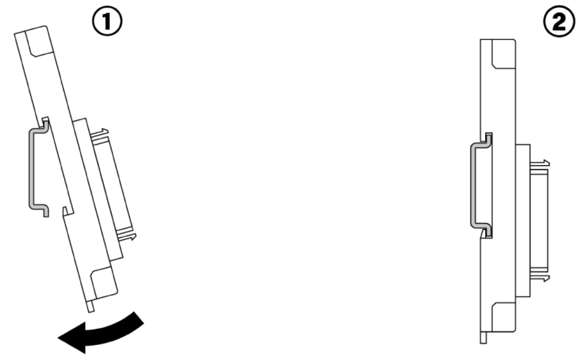
1. **Lightly secure the upper part of the backplane using the mounting holes.**
2. **Align the mounting holes for the lower part and secure.**
3. **Tighten the upper screws.**
4. **Make sure that backplane is securely attached.**



Installation to a DIN Rail

Procedure:

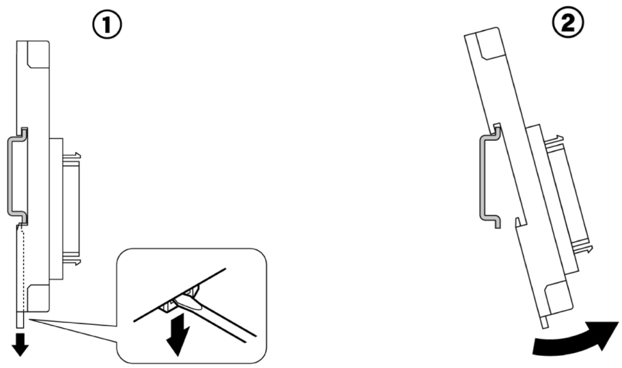
1. **Attach the railing on the rear of the backplane to the DIN rail.**
2. **Push the backplane in the direction of the arrow, as illustrated below, so that it attaches securely.**



Removal from a DIN Rail

Procedure:

1. **Place the tip of a flat-headed screwdriver into the slot for the DIN rail attachment lever.**
2. **Pull out the DIN rail attachment lever with the flat-headed screwdriver and remove the backplane from the DIN rail.**



4.1.2.2 Units

Be sure to install the unit according to the following procedures.

Notes

- **Do not remove the dust proofing label that is attached to the upper portion of the unit until the unit is completely installed and the wiring is completed. However, be sure to remove the dust proofing label prior to operation (☛ section 4.3.3).**
- **Complete the backup battery installation and operation condition switches setting prior to installing the CPU (☛ sections 2.2.1 and 4.1.4).**

1) FP2 backplane

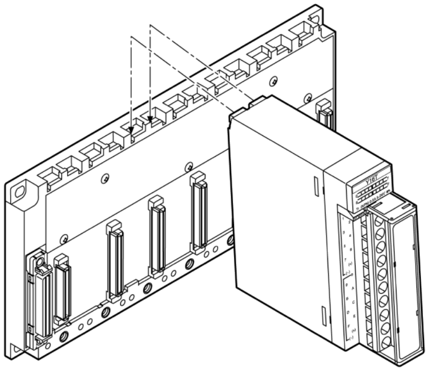
- **With the CPU backplane, install in order from the left to the right, the power supply unit, the CPU, the I/O and the intelligent units.**
  With the expansion backplane, install in order from the left to the right, the power supply unit, the I/O and the intelligent units.
- **Install a power supply unit on to the expansion backplane as well.**
- **Do not install a CPU on to the expansion backplane.**

2) FP2 backplane H type

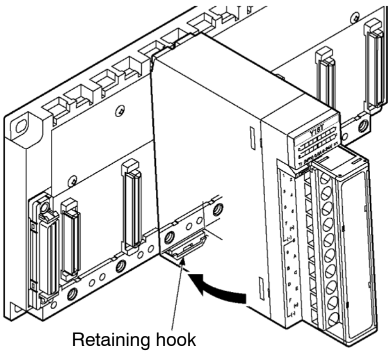
- **The basic FP2 backplane that the CPU unit can be installed and the expansion backplane that other various units can be installed are available.**
- **The positions to install a power supply unit, CPU unit and I/O units are fixed. When using a 1−module type power supply unit, a space of 1 module will be created between the power supply unit and CPU unit, or between the power supply unit and I/O units.**
- **Do not put the wiring in the space in order to prevent the effect of radiation noise.**
- **Set the board No. setting switches on the expansion backplane.**
- **A power supply unit is also necessary on an expansion backplane.**

Procedure:

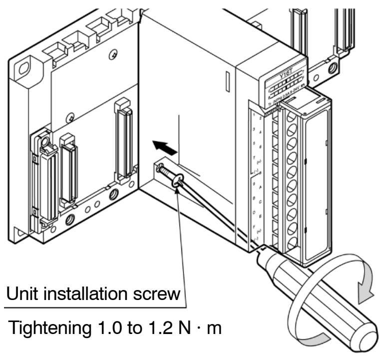
1. **Insert the installation tabs on the rear of the unit into the top of the backplane.**



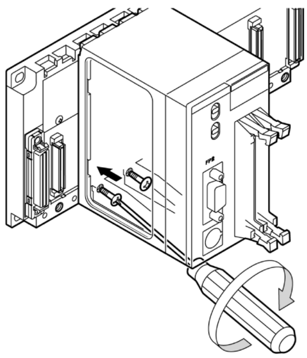
2. **Push the unit in the direction of the arrow and install onto the backplane.**
   When installing the unit to the backplane, make sure the retaining hook firmly clicks into place and that the unit is properly secured to the backplane.



3. **Attach the installation screws and further secure the unit to the backplane. For the 2 modules type unit, there are two installation screws.**



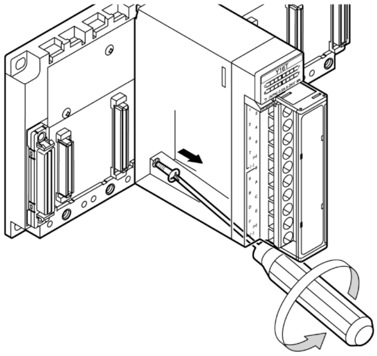
2 modules type unit



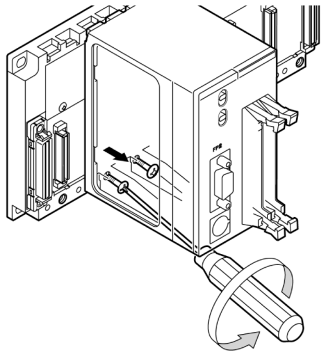
Removing the unit

Procedure:

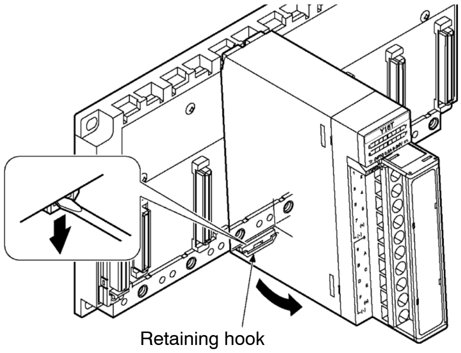
1. Loosen the installation screws.



2 modules type unit



2. Pull out the retaining hook at the bottom of the unit with the tip of a flat-headed screwdriver and remove the unit as illustrated below.



4.1.3 Connecting Expansion Cable

Attaching Connectors

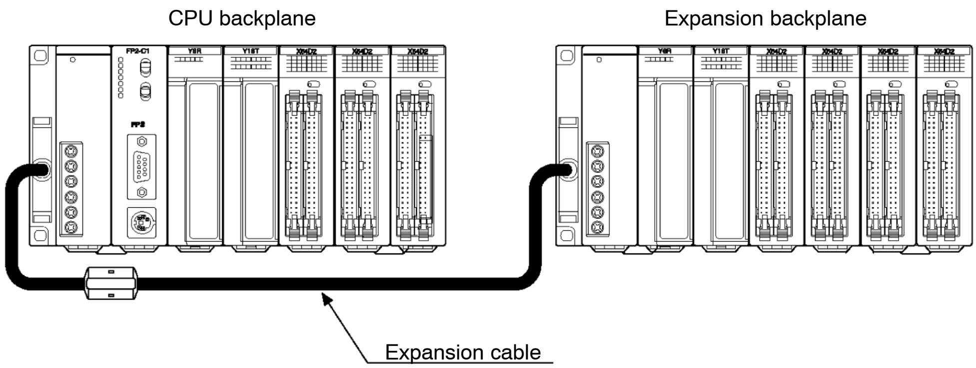
Make sure that the expansion cable is firmly connected.

Do not subject the expansion cable to any twisting or stress.

Connect the expansion cable so that the ferrite core of the expansion cable is situated in close proximity to CPU backplane.

FP2 backplane

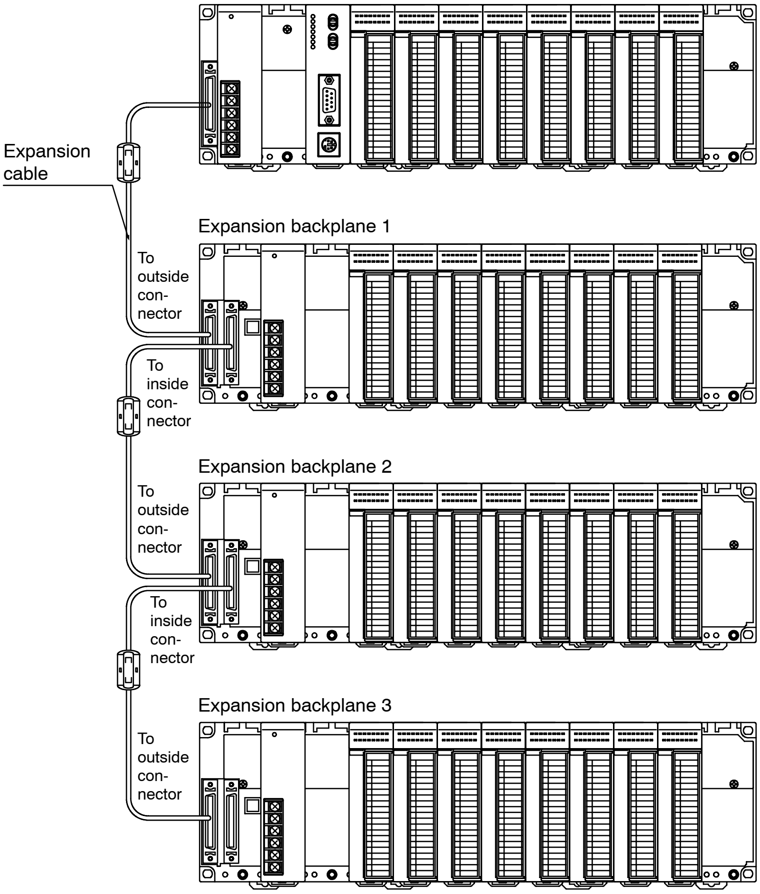
One backplane can be added on for expansion.



FP2 backplane H type

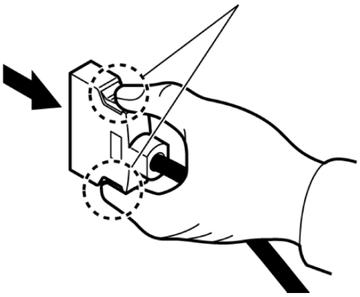
Three expansion backplanes H type can be added on for expansion.

Connect a cable from the connector of the basic backplane to the outside connector of the expansion backplane with the smallest number, and then connect a cable from the inside connector to the outside connector of the next expansion backplane.



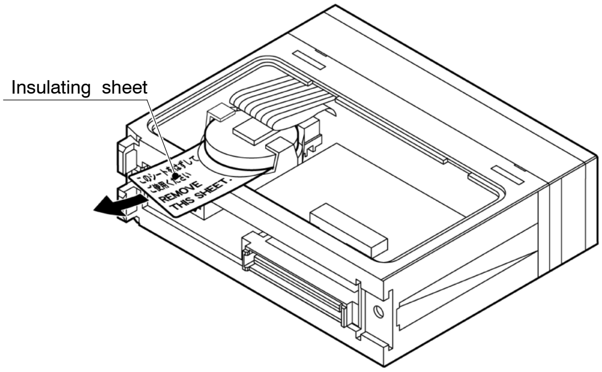
Removing the expansion cable

Hold down the buttons on the side of the connector to release it from the locked condition and pull out the expansion cable.

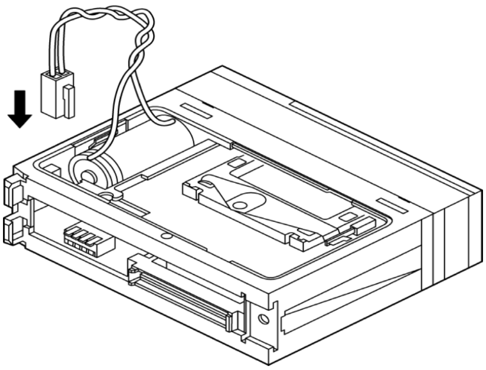


4.1.4 Preparing the Backup Battery

With the FP2, be sure to remove the insulating sheet of the backup battery before installing the CPU onto backplane.



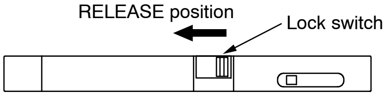
With the FP2SH, connect the connector of backup battery.
Make sure the connector terminals are positioned in the correct directions.



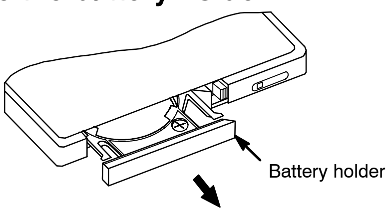
IC memory card: AFP2209

The battery has been removed from the battery holder before shipment. Install the battery before mounting the CPU unit.

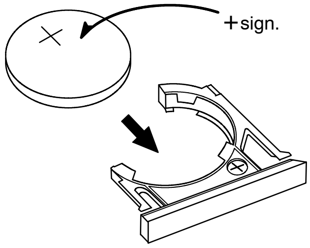
1. **Move to the lock switch to the RELEASE position (toward the battery holder).**



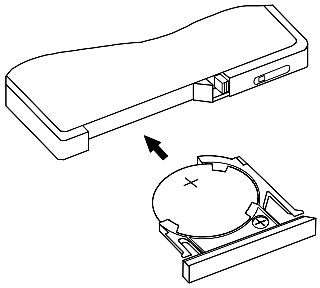
2. **Remove the battery holder.**



3. Place the battery in the battery holder with the side with a '+' sign facing up.



4. Insert the battery holder with the battery all the way seated in the IC memory card.
*** The lock swich is automatically back to the LOCK position when removing the battery holder.**
In this state, insert the battery holder all the way seated.

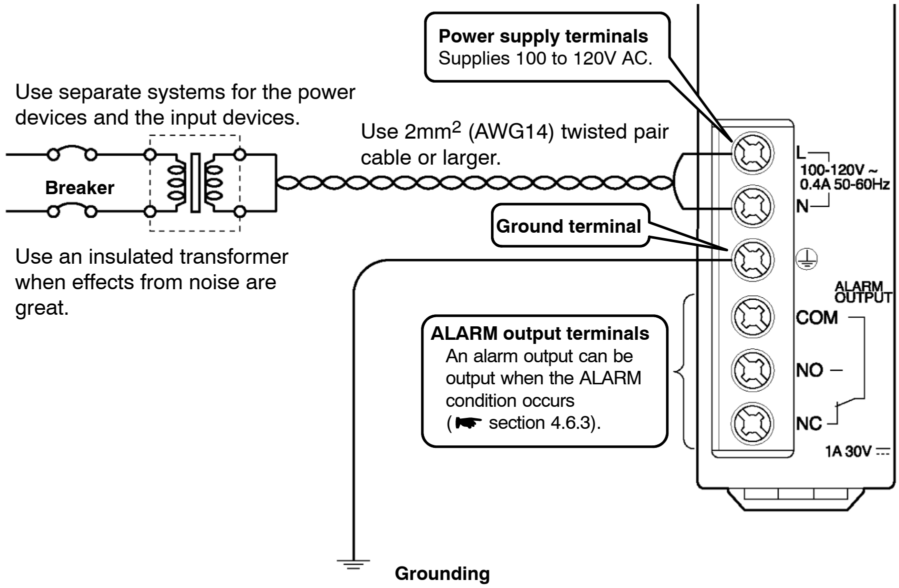


Confirm the lock switch is in the LOCK position.

4.2 Power Supply Wiring

4.2.1 Wiring of Power Supply

Pin layout of power supply unit (FP2−PSA1 is used for the example below.)



Power supply voltage

Verify that the power supply voltage connected to the power supply unit is within allowable limits.

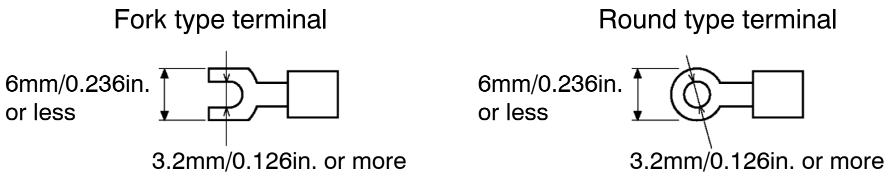
Type	Part number	Rated input voltage	Operating voltage rage	Rated output current
AC type	FP2−PSA1	100 to 120V AC	85 to 132V AC	2.5A
	FP2−PSA2	200 to 240V AC	170 to 264V AC	2.5A
	FP2−PSA3	100 to 240V AC	85 to 264V AC	5A
DC type	FP2−PSD2	24V DC	20.4 to 31.2V DC	5A

Power supply wire

Use power supply wire that is thicker than $2mm^2$ (AWG14) to minimize the voltage drop.

Pressure connection terminal

The following M3 pressure connection terminals are recommended for the wiring.



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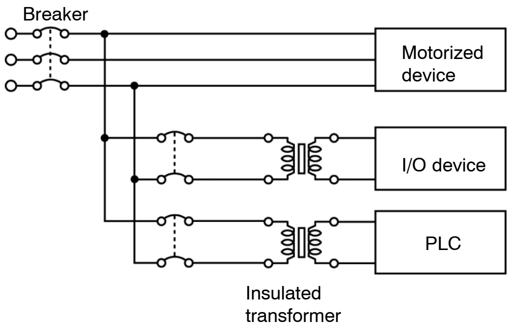
Example of suitable pressure connection terminal

Manufacturer	Shape	Part number	Suitable wire
JST Mfg. Co., Ltd.	Round type	2–N3A	1.04 to 2.63mm^2
	Fork type	2–MS3	Use wire that is thicker than 2mm^2.

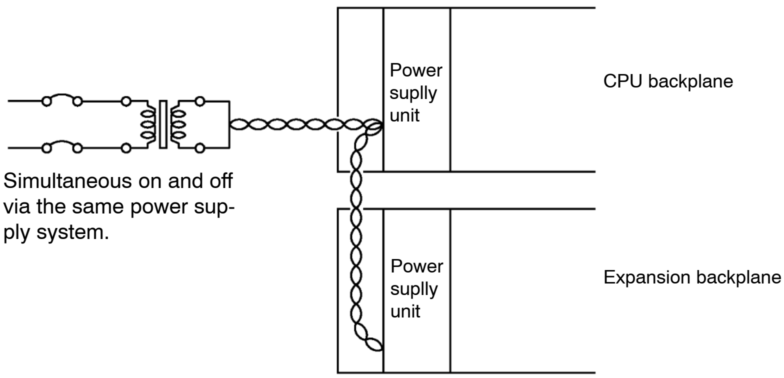
Power supply system

Use separate wiring systems for the FP2/FP2SH power supply unit output devices and motorized devices.



Note

Use the same power supply system for the expansion backplane and CPU backplane so that they are turned on and off simultaneously.



Eliminating effects from noise

Use a low noise power supply

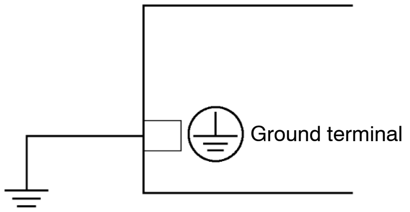
There is sufficient noise resistance for superimposed noise in the power supply wiring, however using an insulated transformer is recommended for further noise protection.

Twist the power supply wire to minimize the effects of noise.

4.2.2 Grounding

Always ground the FP2/FP2SH PLC.

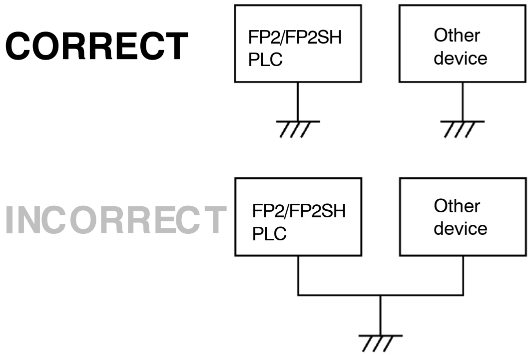
Ground the unit with the ground terminal as illustrated below.



For grounding purposes, use ground wires with a minimum of 2mm^2 (AWG14) and the grounding connection should have a resistance of less than 100Ω.

The point of grounding should be as close to the FP2/FP2SH PLC as possible. The ground wire should be as short as possible.

If two devices share a single ground point, it may produce an adverse effect. Always use an exclusive ground for each device.



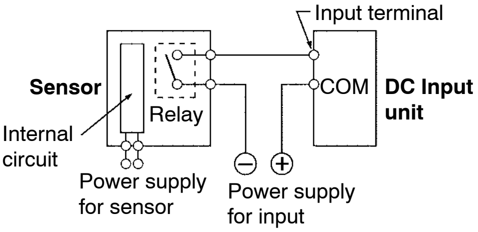
4.3 Wiring Input and Output

4.3.1 Input Wiring

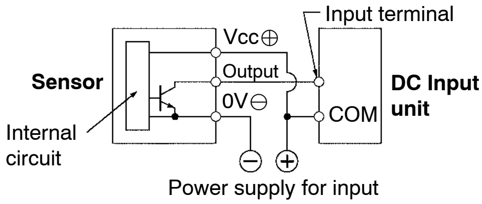
Before the wiring, carefully confirm the specifications for the units to be wired. Specifically, limitations on the ambient temperature and number of points that can be on simultaneously will differ for different units.

Connection of Sensors

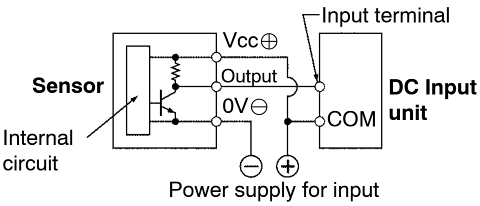
Relay output type



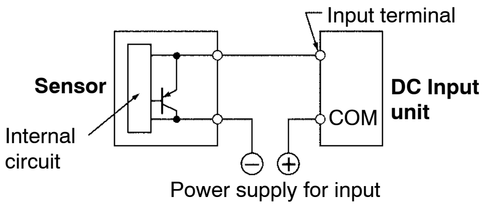
NPN open collector output type



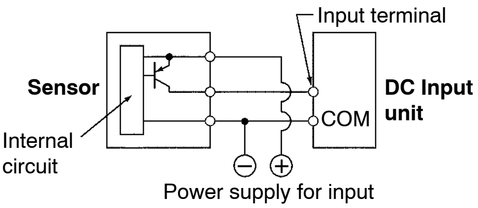
Voltage output type



Two-wire type

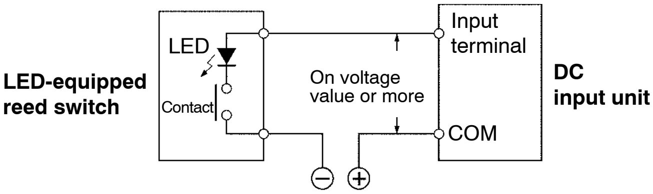


PNP open collector output type



Connection of LED-equipped Reed Switch

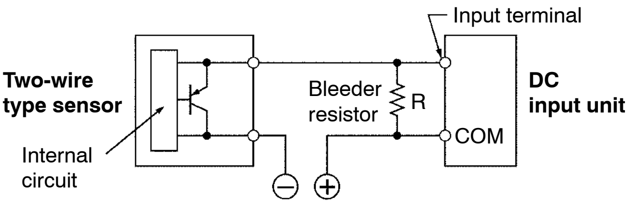
With a LED is connected to an input contact such as LED-equipped reed switch, make sure that the voltage value applied to the input terminal of PLC is greater than on voltage value.
In particular, take care when connecting a number of switches in series.



Connection of Two-wire Type Sensor

If the input of the PLC is not turned off because of leakage current from the two-wire type sensor, the connection of a bleeder resistor is recommended, as shown below.

Using 16-point type DC input unit (FP2−X16D2)
(Off voltage: 2.5V, Input impedance: 3kΩ)



I: Sensor’s leakage current (mA)
R: Bleeder resistor (kΩ)

The off voltage of the input is 2.5V, therefore, select an R value so that the voltage between the COM terminal and the input terminal will be less than 2.5V.
The input impedance is 3kΩ.

The resistance R of the bleeder resistor is: $R \leqq \dfrac{7.5}{3 \times I - 2.5}$ (kΩ)

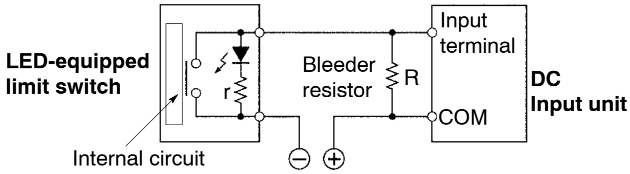
The wattage W of the resistor is: $W = \dfrac{(\text{Power supply voltage})^2}{R}$

In the actual selection, use a value that is 3 to 5 times the value of W.

Connection of LED-equipped Limit Switch

With the LED-equipped limit switch, if the input of the PLC is not turned off or if the LED of the limit switch is kept on because of the leakage current, the connection of a bleeder resistor is recommended, as shown below.

Using 16-point type DC input unit (FP2−X16D2)
(Off voltage: 2.5V, Input impedance: 3kΩ)



r: Internal resistor of limit switch (kΩ)
R: Bleeder resistor (kΩ)

The off voltage of the input is 2.5V, therefore when the power supply voltage is 24V, select R so that

the current will be greater than $I = \dfrac{24 - 2.5}{r}$

The resistance R of the bleeder resistor is: $R \leqq \dfrac{7.5}{3 \times I - 2.5}$ (kΩ)

The wattage W of the resistor is: $W = \dfrac{(\text{Power supply voltage})^2}{R}$

In the actual selection, use a value that is 3 to 5 times the value of W.

4.3.2 Output Wiring

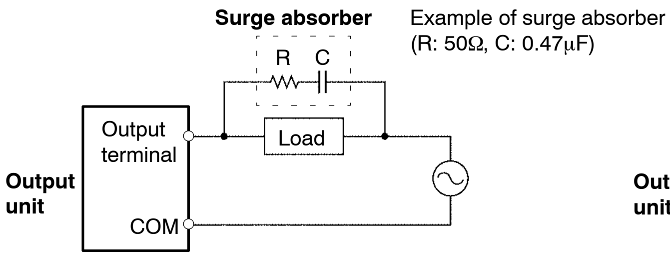
Before the wiring, carefully confirm the specifications for the units to be wired. Specifically, limitations on the ambient temperature, number of points that can be on simultaneously and load current will differ for different units.

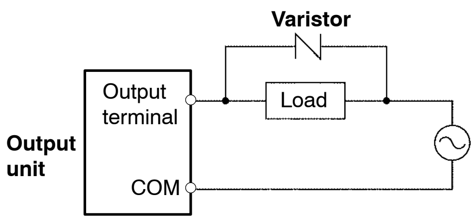
Use a protection circuit when connecting inductive loads and capacitive loads.

Connection of Inductive Loads

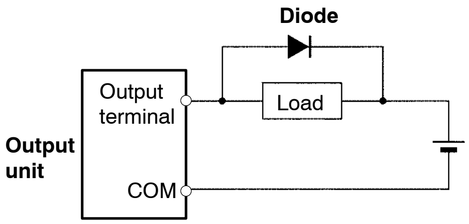
When connecting an inductive load, a protective circuit should be connected in parallel with the load.
When connecting the DC type inductive loads and relay type output unit, be sure to connect a diode for protective circuit across the ends of the load. This will effect the life of the relay.

When using an AC type inductive load



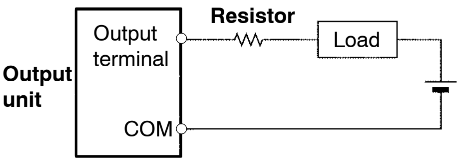


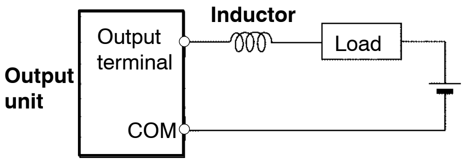
When using a DC type inductive load



Connection of Capacitive Loads

When connecting the loads with large in-rush currents, be sure to connect a protection circuit such as resistor or inductor in series with the load as shown below.





Precautions for Overload

To protect the units from overloading, it is recommended to attach an external fuse for each point. There are times that the elements for the output units cannot be protected even if external fuses are connected.

4.3.3 Cautions Regarding Units

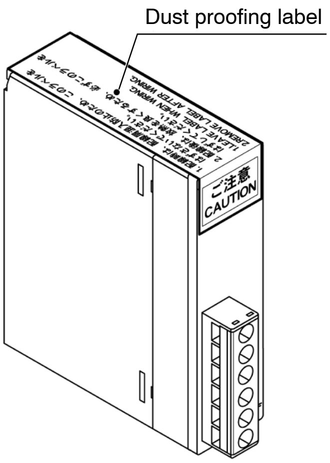
Wiring

Arrange the wiring so that the input and output wiring are separated, and so that the input and output wiring is separated from the power wiring, as so much as possible. Do not route them through the same duct or wrap them up together.

Separate the wires of input/output circuit from the power and high voltage wires by at least 100mm/3.937in.

Dust Proofing Label

Do not remove the dust proofing label that is attached to the upper portion of the unit until the unit is completely installed and the wiring is completed. However, be sure to remove the dust proofing label prior to operation.

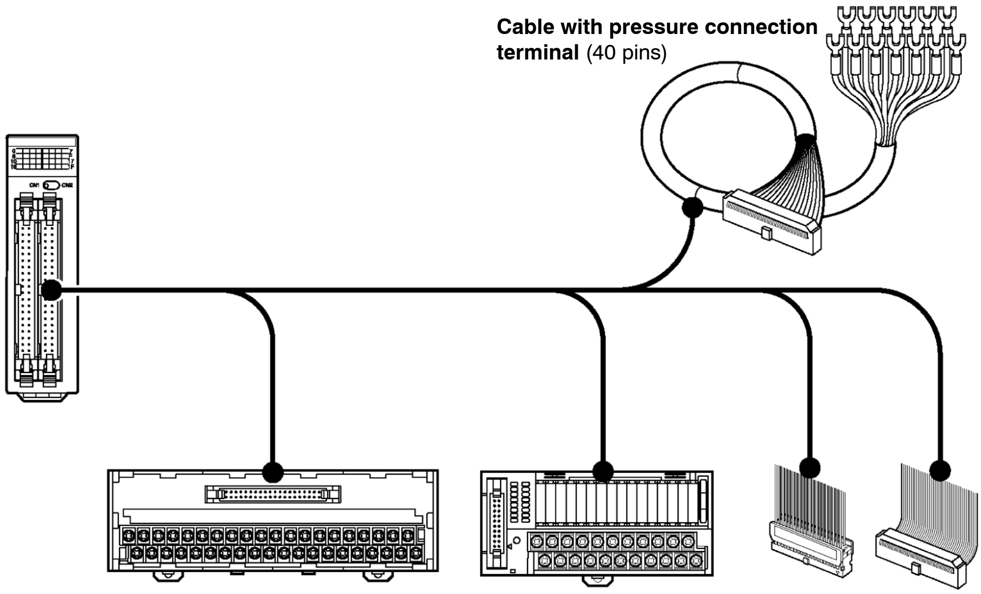


4.4 Wiring the Connector Type I/O Units

4.4.1 Wiring the Connector Type Units

Wiring Method

There are 4 methods for wiring to a connector type I/O unit. Choose the most appropriate method depending on the installation conditions. The set of connector for wire-pressed terminal cable is supplied with the unit.



When using connector for wire-pressed terminal cable(supplied with the unit)
You can directly connect wires from AWG 22 (0.3mm^2) and AWG 24 (0.2mm^2).

Eliminates the bother of wiring connections because the wires can be connected without removing the covers from the wires.

Can correct wiring mistakes easy.

A tool exclusively designed for this purpose is necessary.

For detailed information ☛ section 4.4.2

When using connector and relay terminals
Can be connected using exclusive cables.
With the RT-2 relay terminal, you can control up to 2A.
For detailed information ☛ section 4.4.3

☛ next page

When using cable with pressure connection terminal

The connector converted to a pressure connection terminal using the exclusive cable.

The I/O numbers and corresponding pressure connection terminal pin numbers are the same as for connector terminals on section 4.4.3.

When using flat cable

There is a cable with a connector on only one end.

When using suitable connector, you can use a commercially available flat cable.

For detailed information ☛ section 4.4.4

Table of Connector and Terminal

Number or connector pins				40 pins
Using connector for wire-pressed terminal cable	**Housing**			Supplied with the unit Maintenance part number: AFP2801
	Contact (for AWG22 and AWG24)			
	Semi-cover			
	Pressure connection tool			AXY52000FP
Using terminal	**CT-2 connector terminal**	**DIN rail mounting type**		AYC1140
		Connector terminal cable	**1m/3.281ft.**	AYT51403
			2m/6.562ft.	AYT51405
	RT-2 relay terminal (*Note 2)	**DIN rail mounting type**		AY231502 for input AY232502 for output
		Connector terminal cable	**1m/3.281ft.**	AY15633
			2m/6.562ft.	AY15635
Using cable with pressure connection terminal	**1m/3.281ft.**			AYT58403
	2m/6.562ft.			AYT58405
Using flat cable	**Flat cable with a connector on one end**		**1m/3.281ft.**	AFB8541
			2m/6.562ft.	AFB8542
	Connector only			AFP2802 (40-pin connectors)

☞ Notes

1) **The connectors for wire-pressed terminal cable (40 pins) are supplied with the unit.**

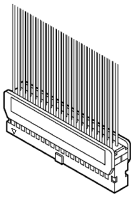
2) **The RT-2 relay terminal cannot be used with PNP collector output type output units (FP2–Y32P, FP2–Y64P, FP2–XY64D2P and FP2–XY64D7P).**

4.4.2 Connecting with Connector for Wire-pressed Terminal Cable

Connector for Wire-pressed Terminal Cable

This is a connector that allows loose wires to be connected without removing the wire's insulation.

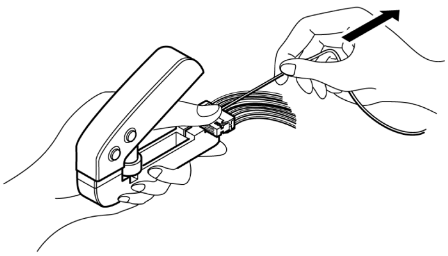
The pressure connection tool is required to connect the loose wires.

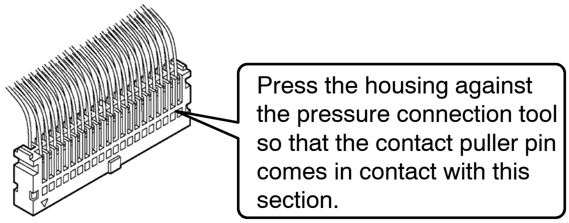


Connector for wire-pressed terminal cable (40 pins)

Rewiring

If there is a wiring mistake or the wire is incorrectly pressure-connected, the contact puller pin provided with the fitting can be used to remove the contact.





Suitable Wires (twisted wire)

Size	Cross section area	Insulation thickness	Remark	Rated current
AWG22	0.3mm^2	dia.1.5 to dia.1.1	Twisted wire of 12 pcs/0.18	3A
AWG24	0.2mm^2		Twisted wire	

Note

The contact suitable for AWG#22 or AWG#24 is supplied with the product. For purchasing a contact suitable for AWG#26 or AWG#28, specify AFP7231FP.

Connector for Wire-pressed Terminal Cable

Unit type	Composition of accessories		
	Housing	Semi–cover	Contact
32–point input unit **32–point output unit**	1 pc	2 pcs	5 pins x 8
64–point input unit **64–point output unit** **32–point input/32–point output unit**	2 pcs	4 pcs	5 pins x 16

Pressure Connection Tool

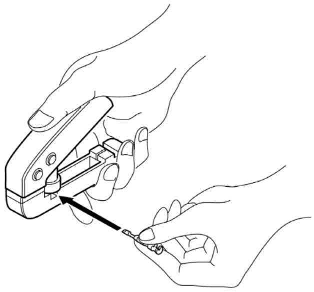
Part number: AXY52000FP

Assembly of Connector for Wire-pressed Terminal Cable

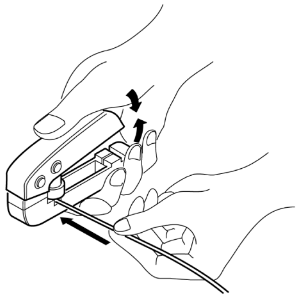
The wire end can be directly press-fitted without removing the wire's insulation, saving labor.

Procedure:

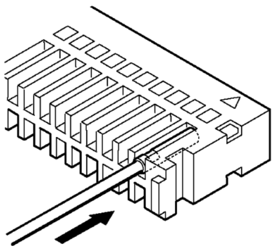
1. **Bend the contact back from the carrier, and set it in the pressure connection tool.**



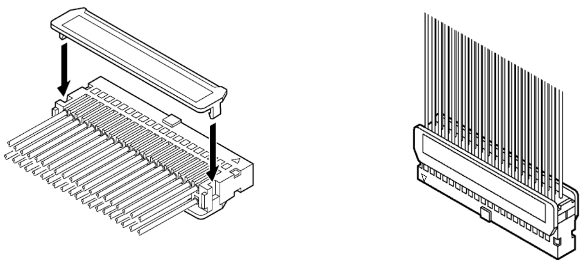
2. **Insert the wire without removing its insulation until it stops, and lightly grip the tool.**



3. **After press-fitting the wire, insert it into the housing.**



4. **When all wires has been inserted, fit the semi-cover into place.**



4.4.3 Connecting the Terminals

CT-2 Connector Terminal

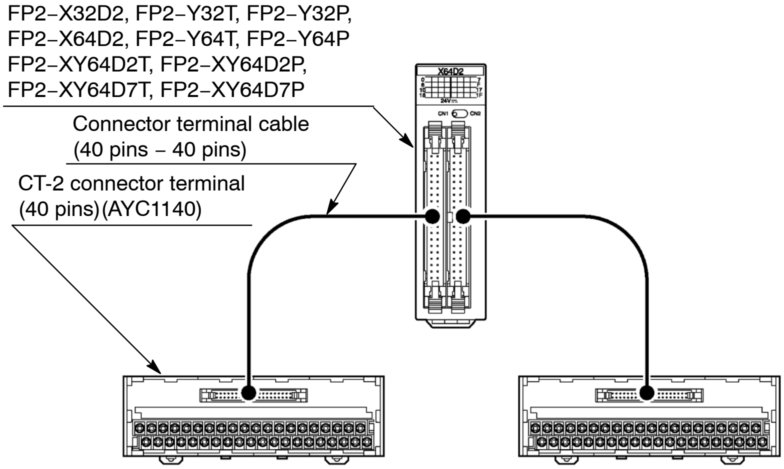
Use a 40-pin type CT-2 connector terminal.

For connecting the terminal to the terminal block, use M3-sized pressure connection terminals.

☞ **Note**

If using the CT-2 connector terminal for the input, connect between the COM terminals.
If using the CT-2 connector terminal for the output, 24V DC should be supplied between (+) and (–) terminals. Power is supplied to drive the internal circuit of the output unit. (Connect between each the (+) terminals and between each the (–) terminals.)

CT-2 connector terminal connection diagram for 32–point type and 64–point type I/O units and I/O mixed units



Correspondence table of 32-point type input unit

When a 32-point type input unit is next to the standard type CPU on the right side.

Terminal number	Input number	Terminal number	Input number
A1	X0	**B1**	X8
A2	X1	**B2**	X9
A3	X2	**B3**	XA
A4	X3	**B4**	XB
A5	X4	**B5**	XC
A6	X5	**B6**	XD
A7	X6	**B7**	XE
A8	X7	**B8**	XF
A9	COM	**B9**	COM
A10	NC	**B10**	NC
A11	X10	**B11**	X18
A12	X11	**B12**	X19
A13	X12	**B13**	X1A
A14	X13	**B14**	X1B
A15	X14	**B15**	X1C
A16	X15	**B16**	X1D
A17	X16	**B17**	X1E
A18	X17	**B18**	X1F
A19	COM	**B19**	COM
A20	NC	**B20**	NC

Correspondence table of 64-point type input unit

When a 64-point type input unit is next to the standard type CPU on the right side.

Examples for the CN1 group

Terminal number	Input number	Terminal number	Input number
A1	X0	**B1**	X8
A2	X1	**B2**	X9
A3	X2	**B3**	XA
A4	X3	**B4**	XB
A5	X4	**B5**	XC
A6	X5	**B6**	XD
A7	X6	**B7**	XE
A8	X7	**B8**	XF
A9	COM	**B9**	COM
A10	NC	**B10**	NC
A11	X10	**B11**	X18
A12	X11	**B12**	X19
A13	X12	**B13**	X1A
A14	X13	**B14**	X1B
A15	X14	**B15**	X1C
A16	X15	**B16**	X1D
A17	X16	**B17**	X1E
A18	X17	**B18**	X1F
A19	COM	**B19**	COM
A20	NC	**B20**	NC

Examples for the CN2 group

Terminal number	Input number	Terminal number	Input number
A1	X20	**B1**	X28
A2	X21	**B2**	X29
A3	X22	**B3**	X2A
A4	X23	**B4**	X2B
A5	X24	**B5**	X2C
A6	X25	**B6**	X2D
A7	X26	**B7**	X2E
A8	X27	**B8**	X2F
A9	COM	**B9**	COM
A10	NC	**B10**	NC
A11	X30	**B11**	X38
A12	X31	**B12**	X39
A13	X32	**B13**	X3A
A14	X33	**B14**	X3B
A15	X34	**B15**	X3C
A16	X35	**B16**	X3D
A17	X33	**B17**	X3E
A18	X37	**B18**	X3F
A19	COM	**B19**	COM
A20	NC	**B20**	NC

Correspondence table of 32-point type output unit

When a 32-point type output unit is next to the standard type CPU on the right side.

Terminal number	Output number	Terminal number	Output number
A1	Y0	**B1**	Y8
A2	Y1	**B2**	Y9
A3	Y2	**B3**	YA
A4	Y3	**B4**	YB
A5	Y4	**B5**	YC
A6	Y5	**B6**	YD
A7	Y6	**B7**	YE
A8	Y7	**B8**	YF
A9	–	**B9**	–
A10	+	**B10**	+
A11	Y10	**B11**	Y18
A12	Y11	**B12**	Y19
A13	Y12	**B13**	Y1A
A14	Y13	**B14**	Y1B
A15	Y14	**B15**	Y1C
A16	Y15	**B16**	Y1D
A17	Y16	**B17**	Y1E
A18	Y17	**B18**	Y1F
A19	–	**B19**	–
A20	+	**B20**	+

Correspondence table of 64-point type output unit

When a 64-point type output unit is next to the standard type CPU on the right side.

Examples for the CN1 group

Terminal number	Output number	Terminal number	Output number
A1	Y0	**B1**	Y8
A2	Y1	**B2**	Y9
A3	Y2	**B3**	YA
A4	Y3	**B4**	YB
A5	Y4	**B5**	YC
A6	Y5	**B6**	YD
A7	Y6	**B7**	YE
A8	Y7	**B8**	YF
A9	–	**B9**	–
A10	+	**B10**	+
A11	Y10	**B11**	Y18
A12	Y11	**B12**	Y19
A13	Y12	**B13**	Y1A
A14	Y13	**B14**	Y1B
A15	Y14	**B15**	Y1C
A16	Y15	**B16**	Y1D
A17	Y16	**B17**	Y1E
A18	Y17	**B18**	Y1F
A19	–	**B19**	–
A20	+	**B20**	+

Examples for the CN2 group

Terminal number	Output number	Terminal number	Output number
A1	Y20	**B1**	Y28
A2	Y21	**B2**	Y29
A3	Y22	**B3**	Y2A
A4	Y23	**B4**	Y2B
A5	Y24	**B5**	Y2C
A6	Y25	**B6**	Y2D
A7	Y26	**B7**	Y2E
A8	Y27	**B8**	Y2F
A9	–	**B9**	–
A10	+	**B10**	+
A11	Y30	**B11**	Y38
A12	Y31	**B12**	Y39
A13	Y32	**B13**	Y3A
A14	Y33	**B14**	Y3B
A15	Y34	**B15**	Y3C
A16	Y35	**B16**	Y3D
A17	Y36	**B17**	Y3E
A18	Y37	**B18**	Y3F
A19	–	**B19**	–
A20	+	**B20**	+

Correspondence table of 32-point input/32-point output type I/O mixed unit

When the I/O mixed unit is next to the standard type CPU on the right side.

Examples for the CN1 group

Terminal number	Input number	Terminal number	Input number
A1	X0	**B1**	X8
A2	X1	**B2**	X9
A3	X2	**B3**	XA
A4	X3	**B4**	XB
A5	X4	**B5**	XC
A6	X5	**B6**	XD
A7	X6	**B7**	XE
A8	X7	**B8**	XF
A9	COM	**B9**	COM
A10	NC	**B10**	NC
A11	X10	**B11**	X18
A12	X11	**B12**	X19
A13	X12	**B13**	X1A
A14	X13	**B14**	X1B
A15	X14	**B15**	X1C
A16	X15	**B16**	X1D
A17	X16	**B17**	X1E
A18	X17	**B18**	X1F
A19	COM	**B19**	COM
A20	NC	**B20**	NC

Examples for the CN2 group

Terminal number	Output number	Terminal number	Output number
A1	Y20	**B1**	Y28
A2	Y21	**B2**	Y29
A3	Y22	**B3**	Y2A
A4	Y23	**B4**	Y2B
A5	Y24	**B5**	Y2C
A6	Y25	**B6**	Y2D
A7	Y26	**B7**	Y2E
A8	Y27	**B8**	Y2F
A9	–	**B9**	–
A10	+	**B10**	+
A11	Y30	**B11**	Y38
A12	Y31	**B12**	Y39
A13	Y32	**B13**	Y3A
A14	Y33	**B14**	Y3B
A15	Y34	**B15**	Y3C
A16	Y35	**B16**	Y3D
A17	Y36	**B17**	Y3E
A18	Y37	**B18**	Y3F
A19	–	**B19**	–
A20	+	**B20**	+

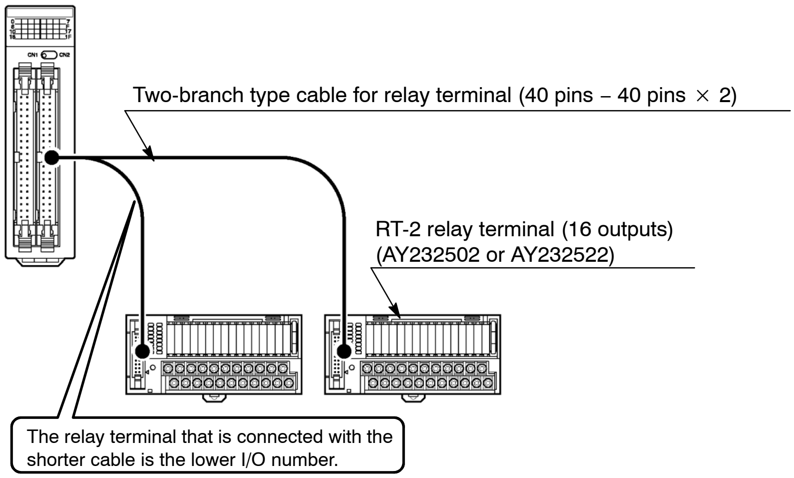
RT-2 Relay Terminal

For 64-point type output unit (FP2−Y64T), you can connect four sets of the RT-2 relay terminals with 16 outputs by using two-branch type cable.

For 32−point type output unit (FP2−Y32T) and output connector side of I/O mixed unit (FP2−XY64D2T, FP2−XY64D7T), you can connect two sets of the RT-2 relay terminals with 16 outputs by using two-branch type cable.

For connecting the terminal to the terminal block, use M3-sized pressure connection terminals.

RT-2 relay terminal connection diagram for 32−point type and 64−point type output units and I/O mixed units



Note

24V DC should be supplied between the (+) and (−) terminals of the relay terminal. Power is supplied to drive the relays of the terminal itself. The I/O power supply supplied to the units and the power supply supplied to the RT-2 relay terminals are the same power supply.

Correspondence table of RT-2 relay terminal

Terminal number	Output number	Terminal number	Output number
0+	Y0	**8+**	Y8
1+	Y1	**9+**	Y9
2+	Y2	**A+**	YA
3+	Y3	**B+**	YB
COM+	COM terminal for Y0 to Y3	**COM+**	COM terminal for Y8 to YB
4+	Y4	**C+**	YC
5+	Y5	**D+**	YD
6+	Y6	**E+**	YE
7+	Y7	**F+**	YF
COM−	COM terminal for Y4 to Y7	**COM−**	COM terminal for YC to YF

4.4.4 Connecting with Flat Cable Connector

When connecting with a flat cable connector, the relationship between the cable number and I/O number is shown below.

Correspondence table of cable number and I/O number

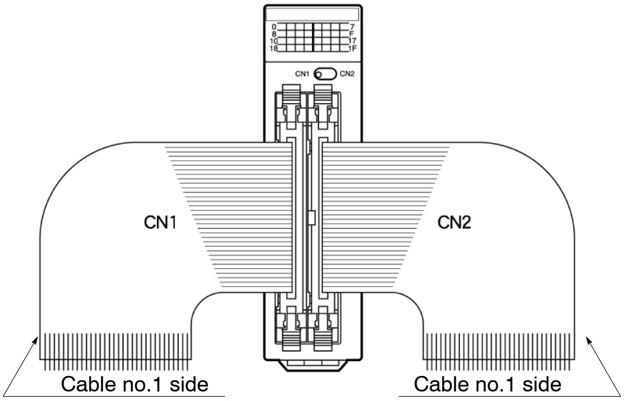
Examples for the CN1 group

Cable No.	Input No.	Output No.	Cable No.	Input No.	Output No.
1	X0	Y0	**21**	X10	Y10
2	X8	Y8	**22**	X18	Y18
3	X1	Y1	**23**	X11	Y11
4	X9	Y9	**24**	X19	Y19
5	X2	Y2	**25**	X12	Y12
6	XA	YA	**26**	X1A	Y1A
7	X3	Y3	**27**	X13	Y13
8	XB	YB	**28**	X1B	Y1B
9	X4	Y4	**29**	X14	Y14
10	XC	YC	**30**	X1C	Y1C
11	X5	Y5	**31**	X15	Y15
12	XD	YD	**32**	X1D	Y1D
13	X6	Y6	**33**	X16	Y16
14	XE	YE	**34**	X1E	Y1E
15	X7	Y7	**35**	X17	Y17
16	XF	YF	**36**	X1F	Y1F
17	COM	–	**37**	COM	–
18	COM	–	**38**	COM	–
19	NC	+	**39**	NC	+
20	NC	+	**40**	NC	+

Examples for the CN2 group

Cable No.	Input No.	Output No.	Cable No.	Input No.	Output No.
1	X20	Y20	**21**	X30	Y30
2	X28	Y28	**22**	X38	Y38
3	X21	Y21	**23**	X31	Y31
4	X29	Y29	**24**	X39	Y39
5	X22	Y22	**25**	X32	Y32
6	X2A	Y2A	**26**	X3A	Y3A
7	X23	Y23	**27**	X33	Y33
8	X2B	Y2B	**28**	X3B	Y3B
9	X24	Y24	**29**	X34	Y34
10	X2C	Y2C	**30**	X3C	Y3C
11	X25	Y25	**31**	X35	Y35
12	X2D	Y2D	**32**	X3D	Y3D
13	X26	Y26	**33**	X36	Y36
14	X2E	Y2E	**34**	X3E	Y3E
15	X27	Y27	**35**	X37	Y37
16	X2F	Y2F	**36**	X3F	Y3F
17	COM	–	**37**	COM	–
18	COM	–	**38**	COM	–
19	NC	+	**39**	NC	+
20	NC	+	**40**	NC	+

Flat Cable Connection Diagram for the 32–point Type I/O Units, 64-point Type I/O Units and I/O Mixed Unit



Flat Cable Connector

Item	Part number
Set of flat cable connector	AFP2802
Flat cable connector (with strain relief, pitch of 1.27mm) (2 pieces)	—

Suitable Wires (twisted wire)

Size	Pitch	Rated current
AWG28 (7pcs./dia.0.127)	1.27mm	1A

4.5 Wiring the Terminal Block Type I/O Units

4.5.1 Wiring the Terminal Block Type Units

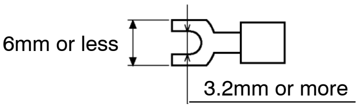
Suitable Wires

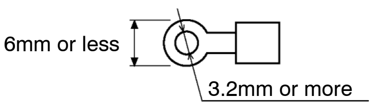
Size	Torque
AWG22 to AWG14 (0.3mm^2 to 2.0mm^2)	0.5 to 0.6N·m

Pressure Connection Terminals

M3.5 terminal screws are used for the terminals. The following pressure connection terminals are recommended for the wiring to the terminals.

Fork type terminal **Round type terminal**



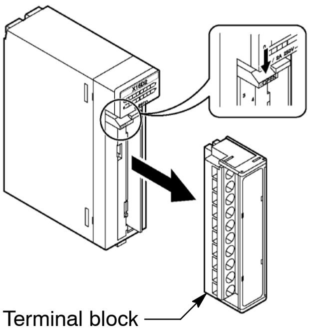


Example of suitable pressure connection terminal

Manufacturer	Shape	Part number	Suitable wire
JST Mfg. Co., Ltd.	Round type	1.25–MS3	0.25 to 1.65mm^2
	Fork type	1.25–B3A	
	Round type	2–MS3	1.04 to 2.63mm^2
	Fork type	2–N3A	

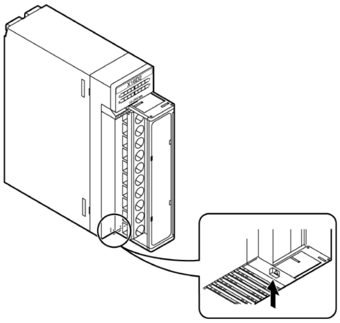
Wiring to Terminal Block

Remove the terminal block before beginning the wiring operations. To remove the terminal block, push downward on the release lever located at the top of the terminal block.



Note

Install the terminal block by inserting it all the way to its original position and pressing the lock button on the bottom of the unit. Then confirm that the terminal block is securely attached and cannot be removed.



Use the numbers described on the terminal cover by replacing with the printed contents of the terminal layout for the main unit.

4.6 Safety Measures

4.6.1 Safety Instructions

Precautions Regarding System Design

In certain applications, malfunction may occur for the following reasons:

Power on timing differences between the PLC system and I/O or motorized devices

An operation time lag when a momentary power failure occurs

Abnormality in the PLC, external power supply, or other devices

In order to prevent a malfunction resulting in system shutdown choose the adequates safety measures listed in the following:

Interlock circuit

When a motor clockwise/counter-clockwise operation is controlled, provide an interlock circuit that prevents clockwise and counter-clockwise signals from inputting into the motor at the same time.

Emergency stop circuit

Add an emergency stop circuit to controlled devices in order to prevent a system shutdown or an irreparable accident when malfunction occurs.

Start up sequence

The PLC should be operated after all of the outside devices are energized. To keep this sequence, the following measures are recommended:

Turn on the PLC with the mode selector set to the PROG. mode, and then switch to the RUN mode.

Program the PLC so as to disregard the inputs and outputs until the outside devices are energized.

☞ **Note**

When stopping the operation of PLC also, have the I/O devices turned off after the PLC has stopped operating.

Alarm function

When an alarm occurs, the PLC turns off the output and stops operation. Even while in this condition, take the appropriate safety precautions outside of the PLC to ensure no malfunction or damage is transmitted to anywhere else in the system.

Grounding

When installing the PLC next to devices that generate high voltages from switching, such as inverters, do not ground them together.

4.6.2 Momentary Power Failures

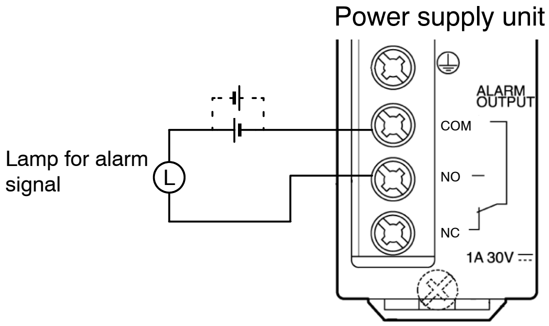
If the duration of the power failure is less than 10 ms, the PLC continues to operate.

If the duration of the power failure is 10 ms or longer, the operation changes depending on the combination of units, the power supply voltage, and other factors. If the PLC continues to operate, the operation may be the same as that for a power supply reset.

The duration of the power failure is the time that the power to the power supply unit stops.

4.6.3 Alarm Output

The alarm output goes on when the watchdog timer is activated by a program error or an error in the hardware itself.
The alarm output terminal has two relay contacts, N.O. (normally open) and N.C. (normally closed). This can be used as an external alarm signal when an error occurs.



Watchdog timer

The watchdog timer is a program error and hardware error detection timer. It goes on when the scan time exceeds 640 ms.
When the watchdog timer is activated, at the same time the ALARM LED lights, the ALARM contacts on the power supply unit go on, all outputs to the output units are turned off and the unit is put in halted state. The system is in a non-processing state that includes communications with programming tools as well.

Note

The ALARM contacts of the power supply unit installed on the expansion backplane will not also operate.

4.6 Safety Measures

Chapter 5

Procedure Until Operation

5.1 Before Turning ON the Power

5.1.1 Check Items

After wiring, be sure to check the items below before turning on the power supply to the FP2/FP2SH system.

Item	Description
Unit mounting status	Does the unit type match the device list during the design stage? Are the unit mounting screws properly tightened? Is the unit dust-protected label detached? Are the installation screws for the expansion memory unit properly tightened? Does the power supply unit type match the actual power supply? Is the lock button for the input/output terminal block properly locked?
Wiring	Are the terminal block mounting screws properly tightened? Does the wiring of terminal match the signal name? Wiring size to small for the current that is carried?
Connection cable	Is the expansion cable properly connected? Is the connection connector properly locked? Is the total length 3.2 m or less? (FP2 backplane H type only)
Setting of CPU	Is the mode selector set to the PROG. mode? Are the specifications for the ROM and RAM correct?
Backup battery of CPU	Has the insulating sheet for the FP2 CPU battery been removed? Is the battery connector for the FP2SH CPU firmly connected?
Expansion backplane	<FP2 backplane H type only> Are the settings of the board No. setting switches correct?
Set of memory backup battery for IC memory card	<AFP2209 only> Is the included battery installed?
Other	Carefully check if there is potential for an accident.

5.1.2 Procedure Up To Operation

After installing and wiring, perform the operation by following procedure.

Procedure:

1. Power on

1) Before turning on the power, check the items described on the previous page.
2) Turn on the power and then, check that the power supply unit's POWER LED and CPU's PROG. LED are on.

2. Enter the program

1) When using a programming tool, perform the operation "Clear Program" before inputting.
2) Enter the program using the programming tool software.
3) Use the programming tool's "total check function" to check for syntax errors.

3. Check output wiring

Use the forced I/O function to check the output wiring.

4. Check input wiring

Check the input wiring by using the input display LEDs or the monitoring function of the programming tool.

5. Trial operation

1) Switch the mode selector from PROG. to RUN mode, check the RUN LED turns on.
2) Check the operation of the program.

6. Edit the program (debug) if necessary

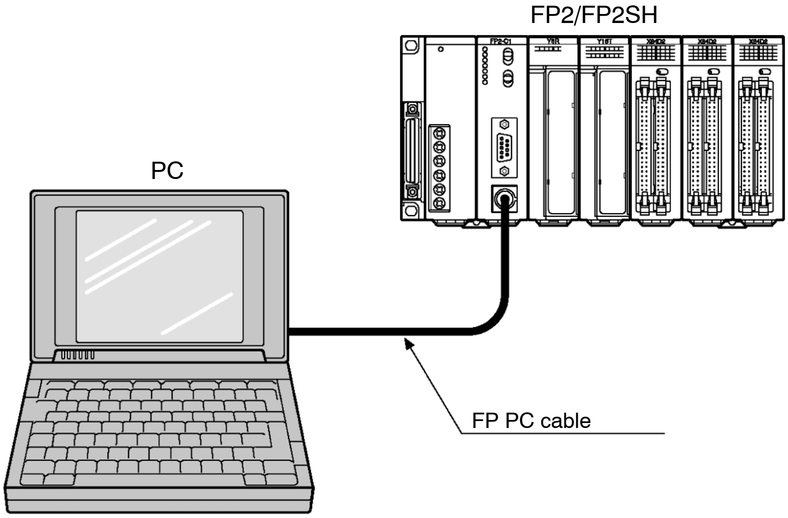
1) If there is an error in the operation, check the program using the monitoring function of the programming tool.
2) Correct the program.

7. Save the edited program

We highly recommend to save the created program onto a floppy disk or hard disk. Printing out is also possible. The program can also be saved on the ROM.

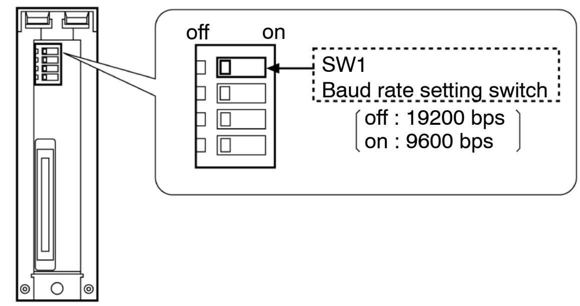
5.2 Programming with Programming Tool Software

5.2.1 Preparations



Setting the baud rate of CPU

The baud rate setting switch is on the rear side of the CPU. Perform the setting with the CPU removed from the backplane.



Set the baud rate of the computer to match that of the CPU.

Connecting the FP2/FP2SH to the computer

Connect using the FP PC cable.

Computer settings

Set to asynchronous. For the setting procedure, refer to the operation manual that came with the computer.

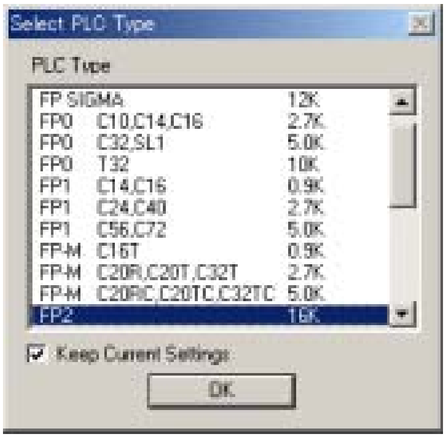
5.2.2 Configuration of Programming Tool Software

Depending on the PLC type and conditions of use, it is necessary to set the basic configuration for programming tool software. Be sure to set these parameters of con-figration before beginning programming.

5.2.2.1 Parameters and Setting Methods

Select PLC type

Select the PLC type that is being used.



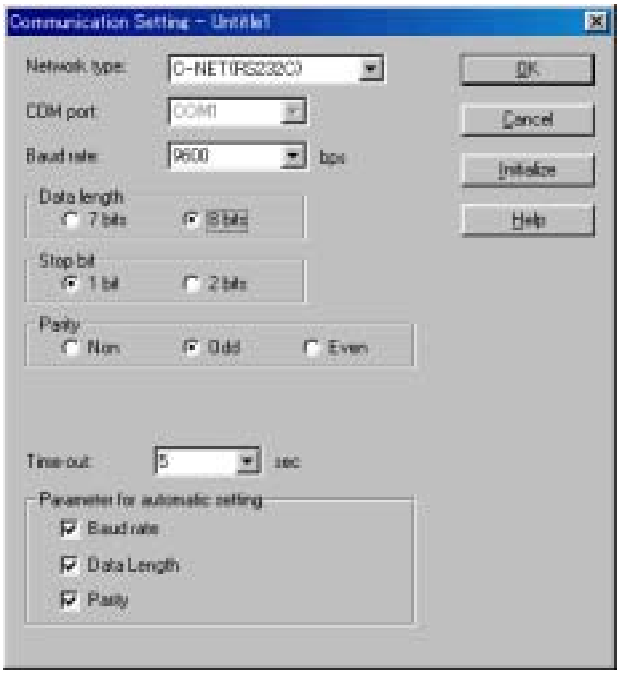
Expansion memory unit used	Selection
None installed	FP2 16k
The FP2–EM1 or FP2–EM7 is installed	FP2 16k
The FP2–EM2, FP2–EM3, or FP2–EM6 is installed	FP2 32k

FP2SH CPU type	Selection
FP2–C2L	FP2SH 32k
FP2–C2, FP2–C2P	FP2SH 60k
FP2–C3P	FP2SH 120k

After your selection, you can change the PLC type.

Communication Settings

Select the Network type or communication format.
In case if RS232C



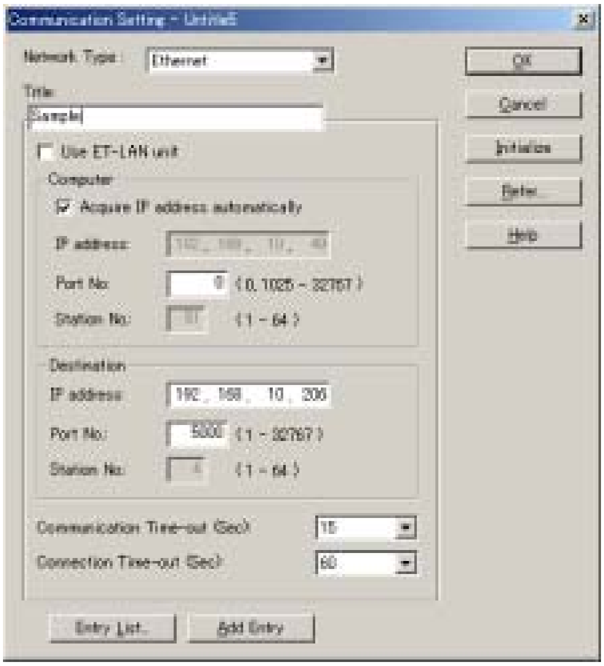
[Baud rate]
PLC default : 9600 bps

[Data length]
PLC default : 8 bits

[Stop bit]
PLC default : 1 bit

[Parity]
PLC default : Odd

In case of Ethernet



For more detail, refer to the FPWIN GR software help.

Chapter 6

FP2/FP2SH Operation

6.1 FP2 Operation

6.1.1 FP2 RAM and ROM Operations

6.1.1.1 Comparison of RAM and ROM Operations

With the FP2, either RAM operation or ROM operation can be selected for the execution method of the program.

RAM operation: Executes the program written into the internal RAM of the CPU.

ROM operation: Transfers the program stored in the ROM of the expansion memory unit to RAM and executes the program.

Comparison of RAM operation and ROM operation

Item	RAM operation	ROM operation
Items necessary for operation	Nothing in particular since operation is performed by the RAM built into the CPU. Normal maximum number of steps is 16k. With the optional expansion memory unit (FP2−EM2, FP2−EM3 or FP2−EM6) installed, the maximum number of steps is 32k.	Optional expansion memory unit (FP2−EM3, FP2−EM6 or FP2−EM7) ROM with the program written on it
Processes inside the CPU	Program written in RAM is executed when RUN mode is entered.	When the power is turned on, the program in ROM is transferred to RAM, and then executed.
Memory contents backed up by battery	Program System registers Hold type data of operation memory	Hold type data of operation memory (The program and the system register within ROM are saved without battery.)
Maintenance	Replacement of backup battery is vital	If program does not use hold type data of operation memory, then operation without a backup battery is possible.

6.1.1.2 Retaining the Data During Power Outages

For the operation memory, such as that for internal relays and data registers, the data that is set as hold-type memory is backed up by the backup battery.

Note

If the internal relays and data registers are set to be non-hold type, then they will not be saved.

Battery-less operation

During ROM operation, if it is not necessary to retain the internal relays and data registers, then you can set them all to non-hold type and perform operation without a backup battery.

6.1.1.3 Setting the Battery Error Warnings

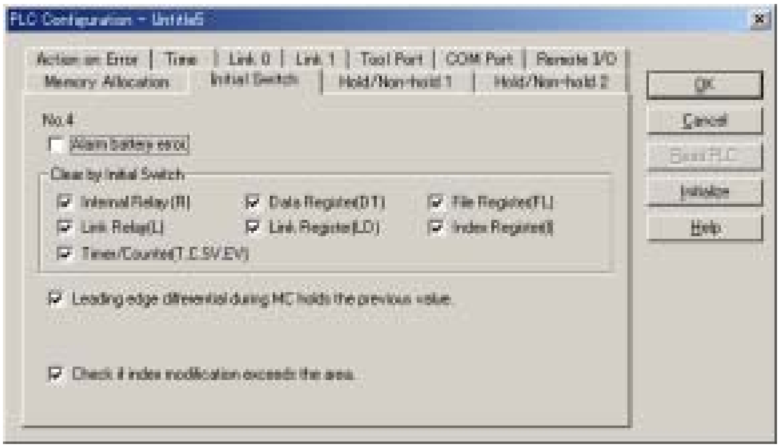
Under normal conditions, if an error occurs with the backup battery, the BATT. and ERROR LEDs on the front of the CPU are on for battery error warning. With ROM operation that does not require the backup battery for operation memory, it is possible to set it so that this warning is not given. With this setting, the BATT. and ERROR LEDs do not light.

Method

The programming tool software is required in order for this setting to be effective.

Procedure:

1. **On the “Option” menu, select “PLC Configuration”.**
2. **Select “Initial Switch” tab.**

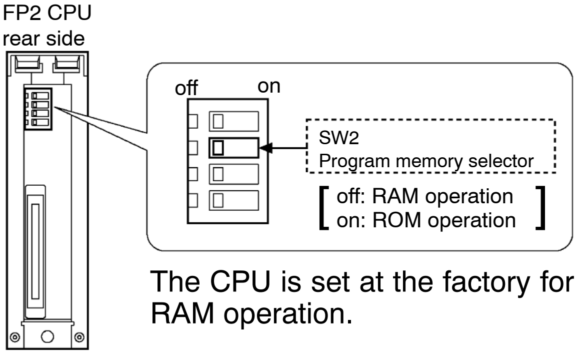


3. **Check “Alarm battery error” off.**

6.2 FP2 RAM Operation

6.2.1 RAM Operation Method

Verify that the operation condition switches (DIP switches) on the back of the FP2 CPU are set for RAM operation (SW2 off).



The CPU is set at the factory for RAM operation.

6.2.2 Precautions When Operating the RAM

The contents written to RAM are all saved by the backup battery. Therefore, it is important to be aware of the life of the backup battery.

Note

Using programming tool software, be sure to copy the program in RAM to the hard disk of the host computer or to a floppy disk.

6.3 FP2 ROM Operation

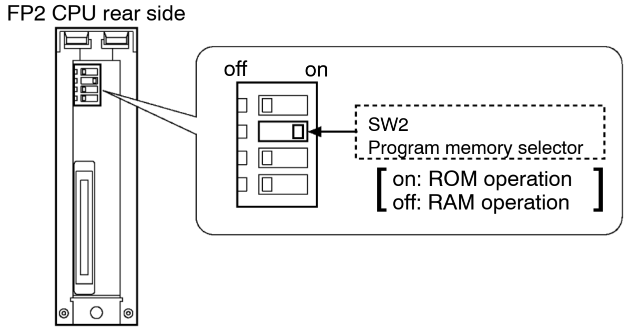
6.3.1 ROM Operation Method

Preparation

Turn off the power supply and remove the CPU from the backplane. Install the expansion memory unit (FP2−EM3, FP2−EM6 or FP2−EM7) to the CPU. Then install the ROM that writes the program to the expansion memory unit. (☛ section 2.3)

Procedure:

1. **Set the operation condition switches (DIP switches) on the back of the CPU for ROM operation (SW2 on).**



2. **Reattach the CPU to the original position on the backplane.**
   When the power supply is turned on, the program in the ROM is transferred to the internal RAM.

☞ **Note**

When the power supply is turned on, the data that was in the RAM will be erased.

6.3.2 Verifying the ROM Contents in RAM Operation

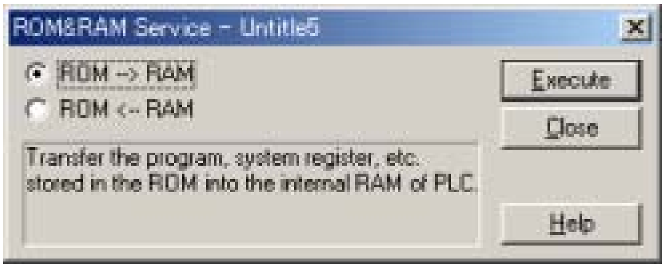
When the operation condition switches (DIP switch) on the rear side of the CPU is set for RAM operation, the CPU reads the contents of the internal RAM. To check the contents of the ROM, you must first copy the contents to RAM by following the procedure below.

Preparation

Have programming tool software ready for use.
Set the CPU to the “PROG.” mode.

Procedure:

1. **On the “Online” menu, select “Online Edit Mode”.**
2. **On the “Tool” menu, select “ROM&RAM Service”.**



3. **Select “ROM −−> RAM” and click “Execute” button.**
   The contents of ROM are copied to the internal RAM.

6.4 Writing to ROM

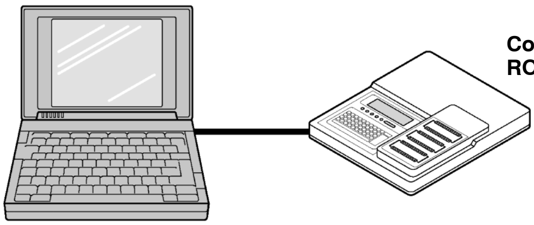
6.4.1 Writing to EPROM Using Programming Tool Software

This method entails using programming tool software at the computer to send the program directly to any commercially available ROM writer and writing the data to the ROM.

Preparation

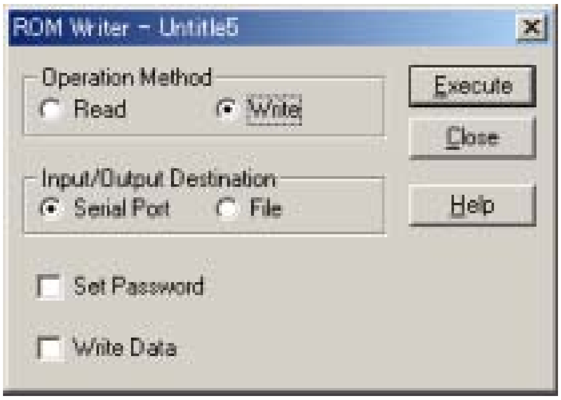
Connect the commercially available ROM writer to the computer.

Attach the optional memory EPROM (FP2−EM5) in the commercially available ROM writer. Read the program with programming tool software.



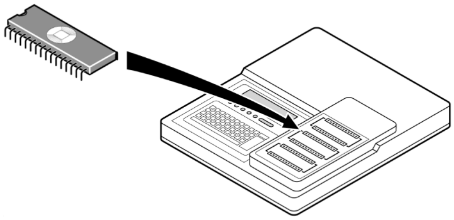
Procedure:

1. **On the “Option” menu, select “Communication Settings”, and set the transmission speed and communication format that matched that for the ROM writer.**
2. **On the “Tool” menu, select “ROM Writer”.**



3. **Select “Write” and “Serial Port” and click “Execute” button. The program is copied to the ROM writer.**

4. **Write the data to the optional memory EPROM (FP2−EM5) with the commercially available ROM writer. The specification of commercially available ROM writer set to EPROM “M27C1001− 12F1 or equivalent” (SGS−THOMSON MICROELECTRONICS).**



6.4.2 Writing to EPROM via FROM

Preparation

Prepare the optional memory FROM (FP2−EM4), the optional memory EPROM (FP2−EM5), and the expansion memory unit (FP2−EM3, FP2−EM6 or FP2−EM7). Also prepare a commercially available ROM writer.

Procedure:

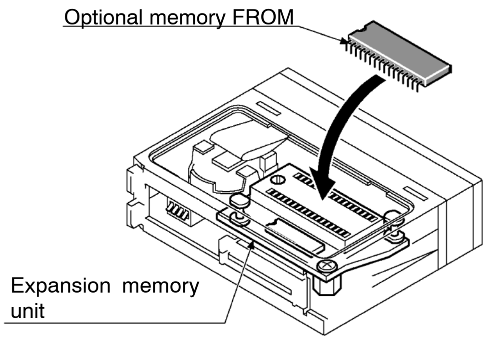
Perform the procedures described in “A” through “D” below. When writing to EPROM, continue on to steps “E”.

A. Passing the program

1. **Pass the program within the CPU.**
   Operations using FPWIN GR
   On the “File” menu, select “Upload from PLC” and read the program from the PLC.
   On the “File” menu, select “Save as” and save the program to a disk.

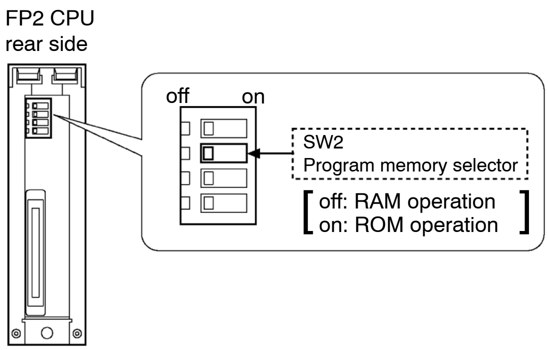
2. **Turn the power off and remove the CPU from the backplane.**

3. **Install the expansion memory unit (FP2−EM3, FP2−EM6 or FP2−EM7) to the CPU. Attach the optional memory FROM (FP2−EM4) to the expansion memory unit.**
   (☛ section 2.3)



FP2 CPU

4. **Verify that the SW2 of operation condition switches (DIP switches) on the back of the CPU are set to RAM operation position (off).**



5. **Reattach the CPU to it original position on the backplane.**

B. Clearing the program within the CPU

☞ **Note**

If inputting of the program is done without first performing this operation, the contents of the internal RAM of CPU may become improper.

Operations using FPWIN GR

1. **On the “Online” menu, select “Online Edit Mode”.**
2. **On the “Edit” menu, select “Clear Program”.**

C. Reading a program from disk

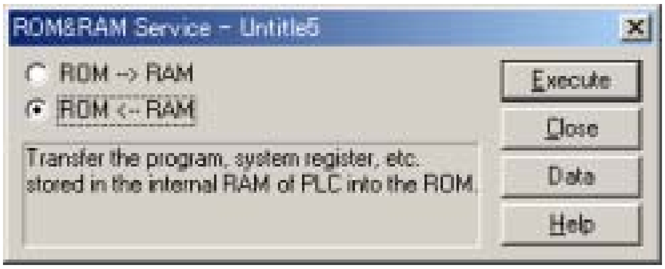
Operations using FPWIN GR

On the “File” menu, select “Open” and load the program from disk.

D. Writing the program from the CPU to the optional memory FROM

Operations using FPWIN GR

1. **On the “Online” menu, select “Online Edit Mode”.**
2. **On the “Tool” menu, select “ROM & RAM Service”.**

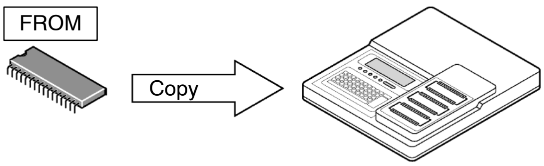


3. **Select “ROM <–– RAM” and click “Execute” button.**

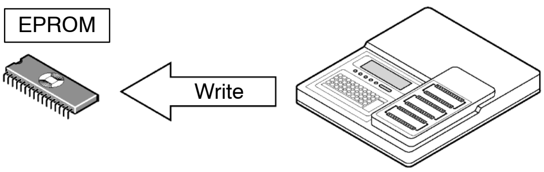
For information on operating the menus, please check the Help menu.

E. Writing to the optional memory EPROM with the ROM writer

1. **Remove the optional memory FROM from the expansion memory unit and install it in the ROM writer.**
2. **Copy the contents of the optional memory FROM to the ROM writer.**



3. **Remove the optional memory FROM and install the optional memory EPROM and write the data to the EPROM.**



6.5 FP2SH Operation

6.5.1 Comparison of RAM, ROM, and IC Memory Card Operation

With the FP2SH, the user can select “RAM operation”, “ROM operation”, or “IC memory card operation” as the method by which programs are to be executed.

RAM operation

Programs written to the RAM in the CPU unit are executed.

ROM operation

With the FP2−C2L or FP2−C2, programs written to the ROM in the expansion memory unit are sent once to the RAM and executed. With the FP2−C2P or FP2−C3P, programs written to the internal FROM are sent once to the RAM and executed.

IC memory card operation (FP2−C2P and FP2−C3P are supported):

Programs written to the IC memory card are sent to the RAM and executed.

Item	RAM operation (SW2: off, SW4: —)	ROM operation (SW2: on, SW4: off)	IC memory card operation (SW2: on, SW4: on)
Items required for operation	None in particular, because the RAM provided as standard in the CPU is used.	With the FP2−C2L and FP2−C2, an optional memory unit and ROM The FP2−C2P and FP2−C3P are built into the FROM.	FP2−C2P or FP2−C3P and IC memory card with the program written to it.
Processing in the CPU	Program in the RAM is executed when the RUN mode is accessed.	When the power supply is turned on, the program in the ROM is sent to the RAM, and the program in the RAM is executed.	When the power supply is turned on, the program in the IC memory card is sent to the RAM, and the program in the RAM is executed.
Contents of memory backed up by battery in the CPU unit	Programs System registers Hold−type data of operation memory Comment data (FP2−C2L, FP2−C2 only)	Hold−type data of operation memory Comment data (FP2−C2L, FP2−C2 only)	Hold−type data of operation memory
Maintenance	Backup battery needs to be replaced.	If the program is in the operation memory and does not use the hold−type memory, operation is possible without a battery.	If the program is in the operation memory and does not use the hold−type memory, operation is possible without a battery. With AIC52000, periodic charging or replacement is necessary. Charging is done by inserting it in the CPU. With AFP2209, the replacement of memory backup battery is necessary.

6.5.2 Retaining Data If the Power Fails

Operation Memory Backup

Of the internal relays, data registers and other operation memories, data specified as hold–type data in the system registers is backed up by the backup battery.

Setting the Alarm Battery Error

Normally, if a problem occurs with the backup battery, the “BATT.” and “ERROR” LEDs on the front panel of the CPU light, to warn of a battery error.

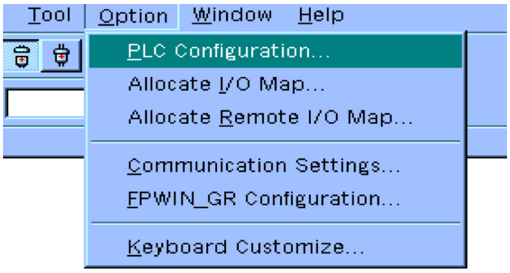
During ROM operation, and when no operation memory backup is required, the alarm battery error can be set to “off”. If this setting is entered, the “BATT.” and “ERROR” LEDs do not light.

Method

The FPWIN GR tool software is used.

Procedure:

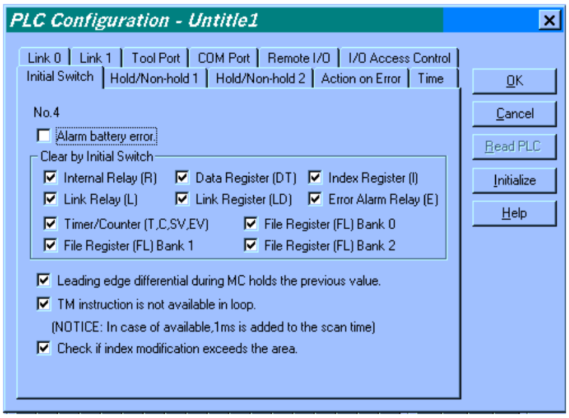
1. **On the “Option” menu, select “PLC Configuration...”.**



The “PLC Configuration” window is opened.

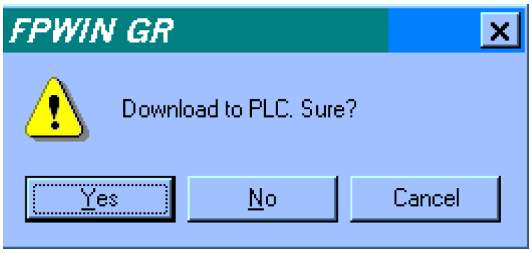
2. Open the “Initial Switch” tab.

3. Delete the check from the “Alarm battery error” check box.



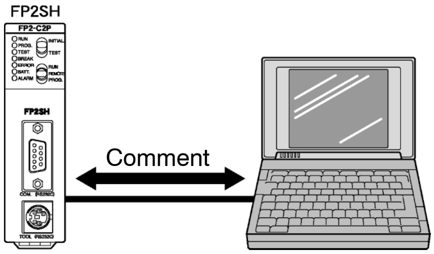
Click on “OK” to close the window.

4. The data is downloaded to the PLC.



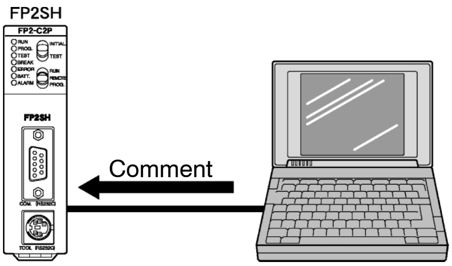
6.5.3 Comment Function

The FP2SH is equipped with a function that allows program comments (I/O comments, block comments, remarks) to be stored.

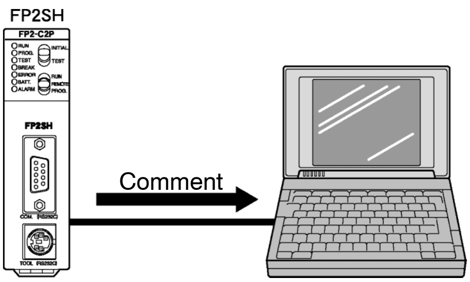


Type	FP2–C2L, FP2–C2	FP2–C2P, FP2–C3P
Storage memory	Internal SRAM	Internal FROM
Storage capacity	128 KB	512 KB
Backup	Backup required	Backup not required

The “Download to PLC” function in the FPWIN GR can be used to write programs and comments. Check to make sure that a check mark has been placed by “Program and Comment” under “Program Access Mode” on the “FPWIN_GR Configuration...” menu of the FPWIN GR.



The “Download to PLC” function in the FPWIN GR can be used to automatically store programs in the FPWIN GR to the internal RAM, and to automatically store comments to the comment memory.

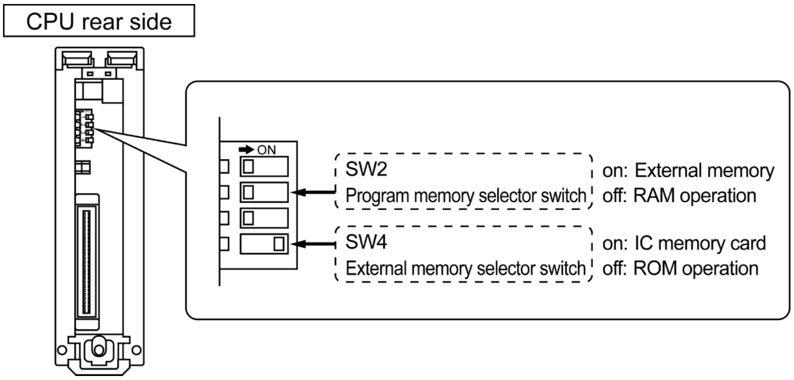


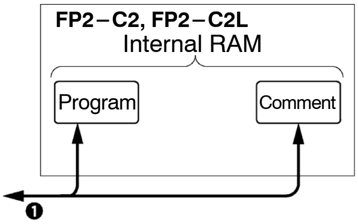
Selecting the “Upload from PLC” function lets you load programs in the internal RAM and data in the comment memory into the FPWIN GR.

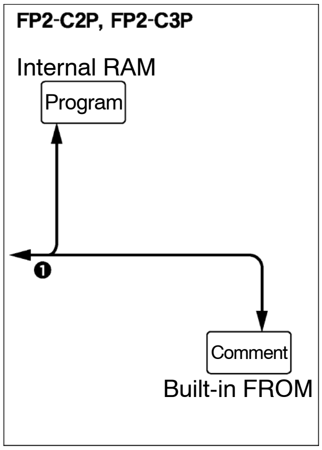
6.6 FP2SH RAM Operation

6.6.1 RAM Operation Method

Check to make sure the DIP switches on the back of the CPU have been set to the RAM operation side (SW2 is off).







Procedure:

1. **Use the tool software to write programs and comments. When doing this, programs are stored in the internal RAM in the FP2SH, and comments are stored in the internal RAM if the FP2−C2 is being used, and in the internal FROM if the FP2−C2P or FP2−C3P is being used.**

2. **RAM operation begins when the PLC is switched to the RUN mode.**

6.6.2 Precautions When Operating the RAM

All contents written to the RAM are retained by the backup battery. Please pay close attention to the service life of the backup battery.

☞ **Note**

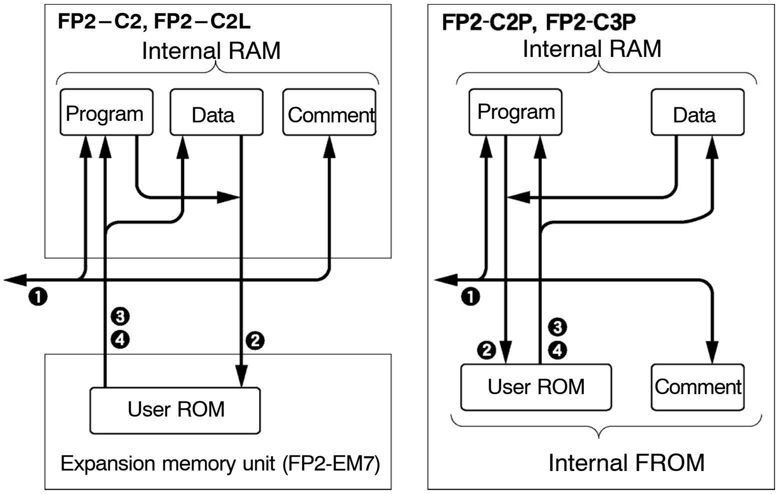
It is recommended to save the programs and data within the CPU in a PC in case that it requires time for the replacement.

6.7 FP2SH ROM Operation

6.7.1 ROM Operation Function

The FP2SH is equipped with a function that causes programs, or programs and data, to be stored in a ROM (FROM or EPROM) that does not require backing up. This function also causes operations to be executed based on the contents of that ROM.

Type	FP2−C2L, FP2−C2	FP2−C2P, FP2−C3P
Storage memory	FROM or EPROM (optional)	Internal FROM
Remark	Memory unit (AFP2208 or FP2−EM7) With the memory unit (FP2−EM7), the master memory (AFP5208) or memory (AFP2509) is required.	FROM is not detachable.



① The “Download to PLC” function in the FPWIN GR can be used to write programs and comments.
In both cases, programs are stored in the internal RAM of the FP2SH.
If the FP2−C2 or FP2−C2L is being used, comments are stored in the internal SRAM. They are not written to the memory unit (AFP2208 or FP2−EM7).
If the FP2−C2P or FP2−C3P is being used, comments are stored in the comment memory of internal F−ROM.

② Programs and data in the internal RAM of the FP2SH are transferred to the user ROM with the “RAM → ROM transfer” function in the FPWIN GR.

③ Programs and data in the user ROM are transferred to the internal RAM of the FP2SH with the “ROM → RAM transfer” function in the FPWIN GR.

④ If the power supply is turned on with DIP switch SW2 set to “on” (SW4: off), programs and data stored in the user ROM are automatically sent to the internal RAM in the FP2SH.

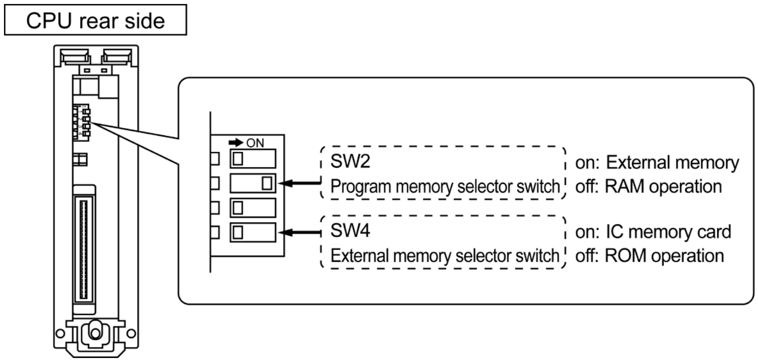
6.7.2 ROM Operation Method

Preparation

Turn off the power supply and detach the CPU.
If using the FP2−C2, insert the expansion memory unit (FP2−EM7) into the CPU, and install the master memory (AFP5208) or the memory (AFP5209) containing the programs.

Procedure:

1. **Set the DIP switches on the back of the CPU to ROM operation (SW2: on, SW4: off).**



2. **Return the CPU to its original position on the backplane. When the power supply is turned on, the contents of the ROM will be transferred to the internal RAM.**

☞ **Note**

Be careful when switching the DIP switches on the back of the CPU. When the power supply is turned on, any contents stored in the RAM up to that point will be lost.

6.7.3 Precautions When Operating the ROM

Precautions Before Turning On the Power Supply

At the point when the ROM is installed, be aware that operation differs as described below, depending on the setting of the DIP switches on the back of the CPU.

If the power supply is turned on when DIP switch SW2 is on and SW4 is off:

When the power supply is turned on, the contents of the memory (ROM) are automatically transferred to the internal RAM and written there. Be aware that the previous contents of the RAM will be lost at that point.

If the power supply is turned on when DIP switch SW2 is off:

Even if the memory (ROM) is installed, the contents of the internal RAM can be read using the programming tools.

Consequently, to confirm the contents of the memory (ROM), the contents of the ROM should be sent to the internal RAM.

To continue using ROM operation, turn off the power supply, and set DIP switch SW2 to the “on” position and SW4 to the “off” position. Then turn the power supply on again.

6.7.4 Checking the ROM Contents While Using RAM Operation

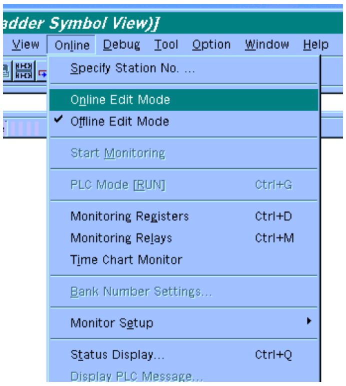
When the DIP switches on the back of the CPU have been set to the RAM operation side, the CPU reads the contents of the internal RAM in that state. To check the contents (programs) of the ROM, use the procedure described below to send the data to the RAM.

Preparation

Set the CPU in the PROG. mode.

Procedure:

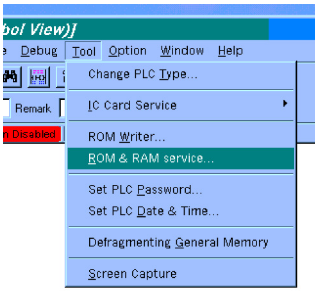
1. Select "Online Edit Mode" on the "Online" menu.



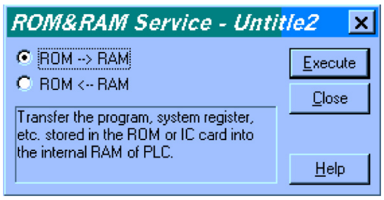
The system goes online, and online monitoring begins automatically.

The  icon on the tool bar can also be used to do this.

2. Select "ROM & RAM service..." on the "Tool" menu.



The "ROM & RAM Service" window opens.



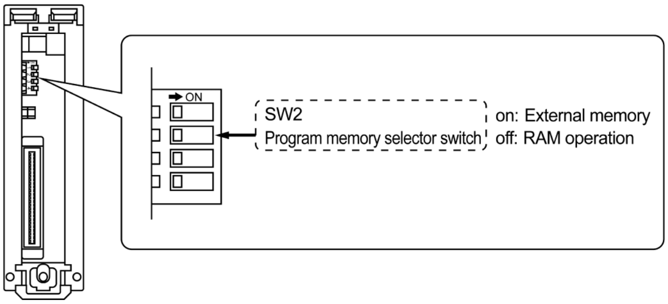
3. The "ROM → RAM" is executed.

Select "ROM → RAM" and click on the "Execute" button.
The contents of the ROM are sent to the internal RAM.

6.7.5 Sending Data from the RAM to the FROM

The “RAM → ROM Transfer” function in the FPWIN GR is used to send programs and data in the CPU to the ROM. The data range can be specified as any of the following fields: WL, WR, DT, FL, SV, EV, and LD.

CPU rear side

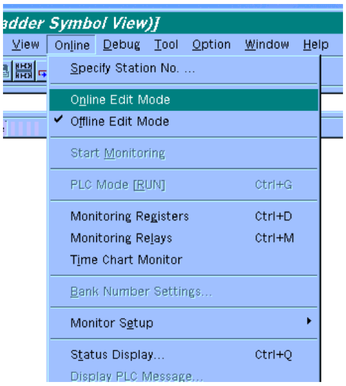


Preparation

Set the CPU in the PROG. mode.

Procedure:

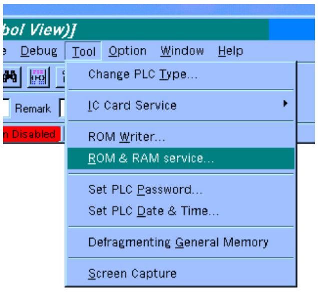
1. **Select “Online Edit Mode” on the “Online” menu.**



The system goes online, and online monitoring begins automatically.

The  icon on the tool bar can also be used to do this.

2. **Select “ROM & RAM service...” on the “Tool” menu.**



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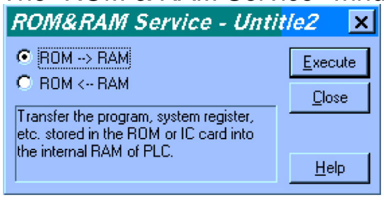
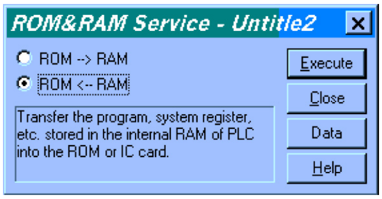
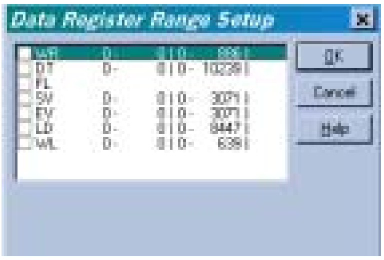
The “ROM & RAM Service” window opens.



3. Select “ROM ← RAM” and press the “Data” button.



The “Data Register Range Setup” window opens.



4. Select the data and specify the range.
Clicking on the check box in front of the data type specifies whether or not that data can be sent. Data marked with a check mark can be sent.
To specify the range, double–click on the list.

Storage Capacity of User ROM

The potential storage capacity of user ROM is:

	Number of program step
	Fixed value (2k words)
+	Data capacity
	Total number of words

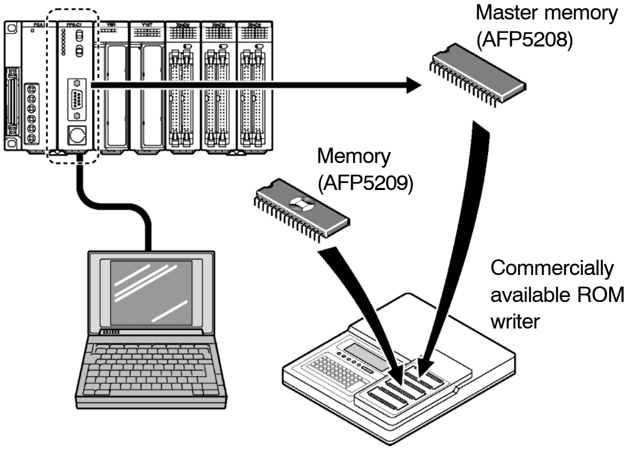
The largest total value of the above is 128k words.

Precautions for Comment Storage

Editing of the program cannot be done during ROM operation. Transfer the data after set the DIP switches SW2 to off.

6.7.6 Writing Data to the ROM (AFP5209) (only the FP2−C2 can be installed)

The master memory is a flash ROM, and data can be written to it when it is installed in the CPU. However, data can only be written when the memory is an EPROM and when a commercially available ROM writer is used.



Procedure of Writing to Memory (AFP5209) Using Master Memory (AFP5208)

1. **Turn the power off and install the expansion memory unit (FP2−EM7) installed with the master memory (AFP5208) to CPU. Turn off the DIP switches SW2 of CPU.**
2. **Verify that the PROG. mode has activated and turn the power on.**
3. **Using the “RAM → ROM” function of the FPWIN GR tool software, transfer the contents of the internal RAM to master memory.**
4. **Turn the power off and detach the master memory from the CPU. Attach it to the commercially available ROM writer.**
5. **Transfer the contents of master memory to the commercially available ROM writer.**
   The ROM writer settings should be specified as those for the M27C2001 (SGS−TOMSON).
6. **Remove the master memory (AFP5208), install the memory (AFP5209), and write the data. The ROM writer settings should be specified as those for the M27C2001 (SGS−TOMSON).**

☛ next page

☞ Notes

- **Refer to the commercially available ROM writer manual regarding the ROM IC type setting and writing method. If a passwords is on the CPU, it is possible to create a password for master memory.**
- **When writing the contents of the FP2SH internal RAM to master memory, be sure to verify that the DIP switches SW2 is off position before turning the power on.**

☞ Notes

1) The above explanation describes the case where the memory unit is used in combination with F−ROM and EP−ROM. As the nonvolatile memory has been implemented in the memory unit (Model number AFP2208), a commercial ROM writer cannot be used for writing.

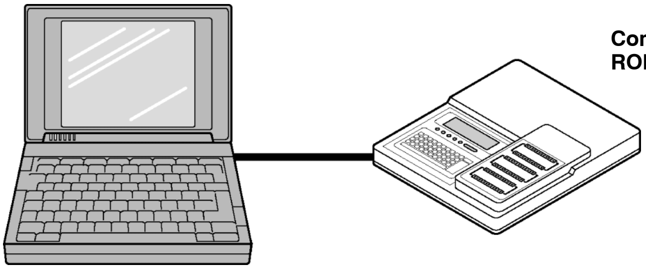
2) The parts for the optional memory to be used differ depending on FP2 or FP2SH.

6.7.7 Writing Data to the ROM: Using the FPWIN GR

With this method, programs are sent directly from the personal computer (FPWIN GR tool software) to the ROM writer, and are written to the ROM. With the FP2SH, this method can be used only when the expansion memory unit (FP2−EM7) is used in combination with the FP2−C2 CPU.

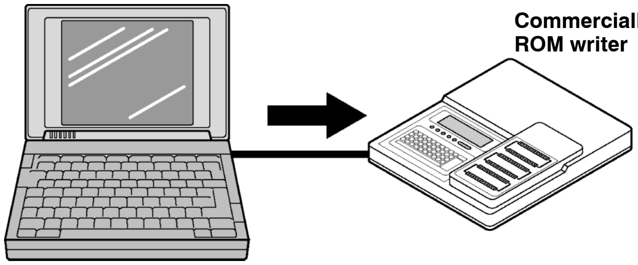
Preparation

Connect the personal computer and the ROM writer.



Procedure:

1. **On the "Tool" menu of the FPWIN GR tool software, select "ROM Writer" to display the dialog box for the ROM writer.**
2. **Specify "Write" as the "Operation Method" and "Serial Port" as the "Input/Output Destination", and click on "Execute".**
   The program is sent to the ROM writer.

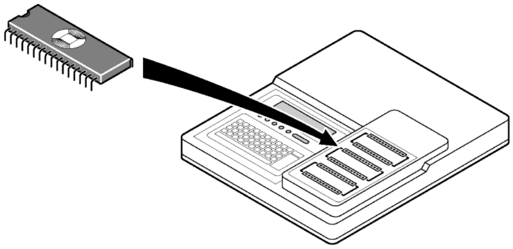


☞ **Note**

In the ROM writer settings, the flow control (X−on/off) should be turned on.

☛ next page

3. Install the memory in the commercially available ROM writer and write the data.
The ROM writer settings should be specified as those for the M27C2001 (SGS−TOMSON).



Notes

- **Refer to the commercially available ROM writer manual regarding the ROM IC type setting and writing method.**
- **It is possible to create a password for master memory.**

6.8 FP2SH IC Memory Card Operation (for FP2−C2P/ FP2−C3P)

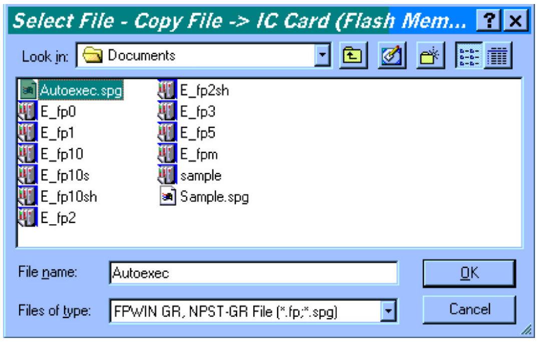
6.8.1 Operating Using the IC Memory Card

IC memory cards can be used to back up programs and as operation memories, but they can also be used for operation, with programs that have been written to the card.

Writing Programs to the Card

The “Copy File” menu in the tool software is used to write programs to a card. When this is used to transfer programs automatically, a file created ahead of time must be converted to the file to be used for automatic transfer.

The converted file can be confirmed in the software, under the file name “Autoexec.spg”.



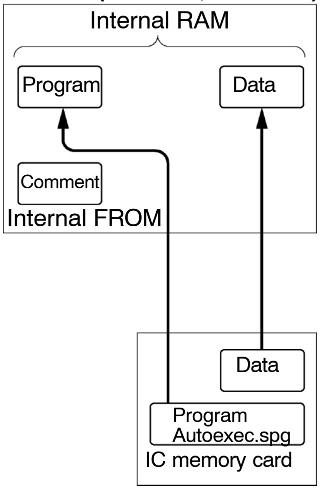
If the card is an SRAM type, the “ROM & RAM service...” menu and “IC Card Service” menu can also be used.

Executing Programs

There are two ways to execute programs written on IC memory cards, described below.

① **Programs are automatically transferred when the power supply is turned on.**
If the power supply is turned on when the DIP switches on the back of the CPU are set so that both SW2 and SW4 are on, the “Autoexec.spg” file stored in the IC memory card is sent to the internal RAM. When the mode is switched to RUN, operation begins in accordance with the contents of that file.

FP2SH (FP2-C2P, FP2-C3P)



② **Sending programs from the “ROM & RAM service...” menu**
If the power supply is turned on when the DIP switches on the back of the CPU are set so that SW2 is off and SW4 is on, executing the “ROM → RAM” operation causes the “Autoexec.spg” file stored in the IC memory card to be sent to the internal RAM. When the mode is switched to RUN, operation begins in accordance with the contents of that file.

Before the “ROM → RAM” menu is executed, any contents loaded with the tool become the contents of the internal RAM.

6.8.2 Creating Files for Automatically Run Programs

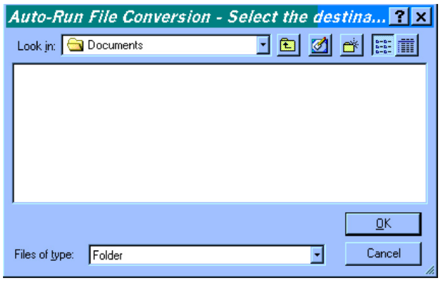
In order to automatically execute programs stored on the card when the power supply is turned on, the following procedure must be used to convert the programs to programs that will run automatically.

Procedure:

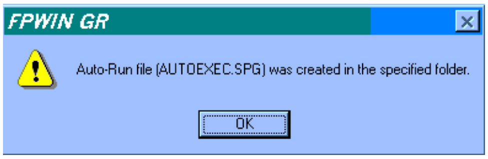
1. **On the FPWIN GR tool software menu, select the following: “Tool” ∍ “IC Card Service” ∍ “Auto−Run File Conversion...”.**

2. **Select the program to be started up automatically.**

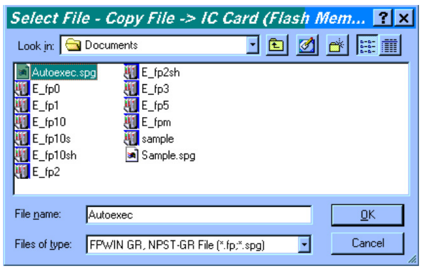
3. **Select the destination to which the program is to be stored after it is converted.**



4. **An auto run file is created, and a confirmation message displayed.**



The auto run file created in this procedure can be read using the various IC card menus. The following shows the screen displayed for “Copy File to IC Card (Flash Memory)”.



6.8.3 How the IC Memory Card is Operated

Turn off the power supply, and remove the CPU.
Have the IC memory card ready that contains programs already written to it.

Procedure:

1. **Set the DIP switches on the back of the CPU for IC memory card operation (SW2: on, SW4: on).**
2. **Install the CPU back in its original position on the back-plane.**
   If the power supply is switched on in the RUN mode, the program on the IC memory card called "Autoexec.spg" is sent to the internal RAM. The program is transferred at the point when the power supply is turned on.

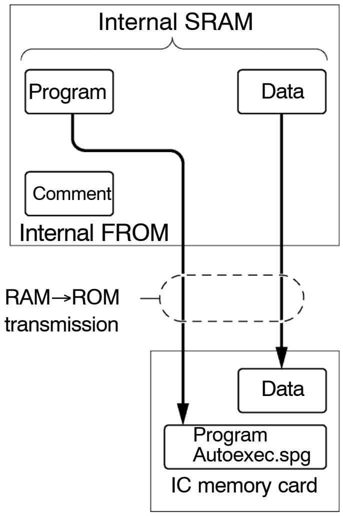
☞ **Note**

If the power supply is turned on with the "Autoexec.spg" file on the IC memory card, all contents of the RAM up to that point are lost.

6.8.4 Transferring Data From the RAM to the IC Memory Card

The “RAM → ROM Transfer” function in the FPWIN GR tool software is used to send programs and data in the CPU to an SRAM type IC memory card. The data range can be specified as any of the following fields: WL, WR, DT, FL, SV, EV, and LD. (DIP switch settings: SW2: off, SW4: on)

FP2SH (FP2-C2P, FP2-C3P)



Note

This method can only be used with an SRAM type IC memory card.

6.8 FP2SH IC Memory Card Operation (for FP2−C2P/FP2−C3P)

Chapter 7

IC Memory Card

7.1 Using the IC Memory Card

7.1.1 Types of IC Memory Cards

There are two types of IC memory cards, an SRAM type and an FROM type. The user can select the appropriate type for the application at hand.

Type	Memory capacity	Part number
FROM type	2MB	AIC50020
SRAM type	2MB	AIC52000
		AFP2209

FROM type

No battery backup is required, so this type is ideal for saving programs.
Programs are written using the “Copy File to IC Card...” function in the FPWIN GR.
When used as an expansion memory, this type is a read–only card. The “Data Editor” is used to write data.

SRAM type

This is ideal for use in expanding the data memory area. When used as an expansion memory, the F13(ICWT) instruction and F12(ICRD) instruction of the sequence program are used to write and read data automatically.

About AFP2209

An interchangeable lithium battery is used.
When you use for the first time, install the battery included.
The battery voltage of IC card is detected only once when the CPU unit is powered on.
An error will not be determined if the battery is replaced during power–on.

About AIC52000

An internal secondary battery is provided for backup purposes.
The data on the SRAM type IC memory card is backed up by a chargeable secondary battery.
When the card is first inserted in the CPU and the power supply is turned on, the battery is not charged, so an error reading “IC card battery error” occurs. Before using the card for the first time, always insert it in the CPU and leave it for at least 24 hours before turning on the power supply. (This fully charges the battery.)

Memory backup time (Ambient temperature of 25 °C)

Model No.	Memory retention time	The battery life
AFP2209	Approx. 3 years or more	
AIC52000	3 months	If operated at 25 °C for 12 hours a day with the power supply off, : Approx. 10 years The service life is shorter at high temperatures, or if the power supply is left off or long periods of time.

7.1.2 Using the IC Memory Card

The IC memory card is available as an optional memory for the FP2−C2P/FP2−C3P. (It cannot be used with the FP2−C2.)
IC memory cards can be used for two types of applications: saving programs and expanding the data memory area. Also, a single IC memory card can be used in the following three ways:

Only for saving programs

Only for expanding the data memory area

For both saving programs and expanding the data memory area

Using the Card to Save Programs

Sequence programs can be written to IC memory cards and saved on them. The IC memory card with the program written to it is then used as a program memory.

If the FPWIN GR or a similar tool is used to change the file name to “Autoexec.spg”, as an auto run file, and the file is copied or the program is transferred, and if the DIP switches on the CPU are set so that SW2 and SW4 are both on, the program can be automatically transferred to the RAM at the same time that the power supply is turned on.
If the **F14 (PRGRD)** instruction is executed in the RUN mode, a program can be substituted for another program in any desired file.
If an SRAM type of IC memory card is being used, the “ROM & RAM service” in the FPWIN GR can be used to copy the contents of the RAM in the CPU to the IC memory card.

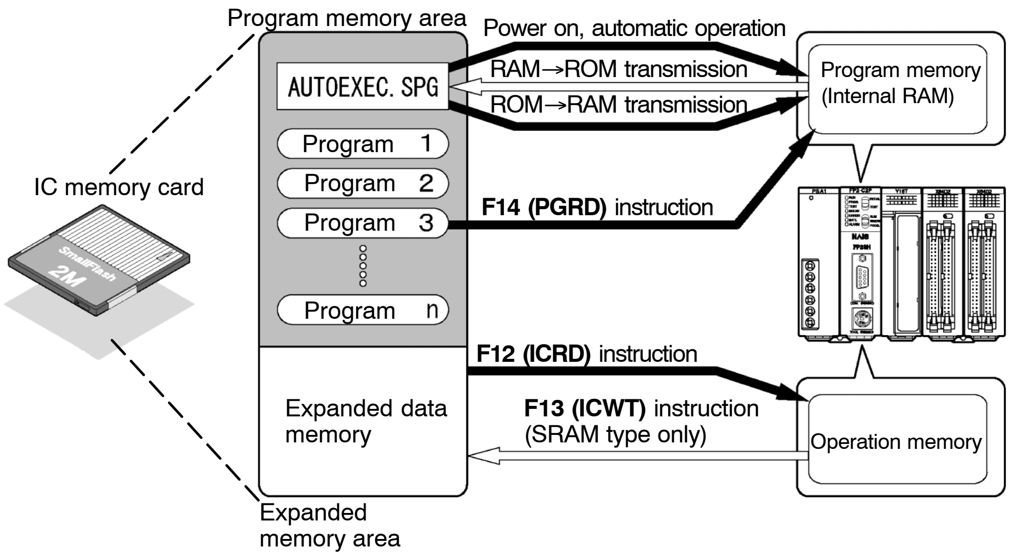
If the card is being used as a program memory, there are four ways to read programs from the card, described below:
Programs can be automatically read when the power supply is turned on.
Programs can be read using the “ROM & RAM service” menu on the FPWIN GR.
Programs can be read using the “Upload Program from IC Card...” menu on the FPWIN GR.
The **F14 (PRGRD)** instruction of the sequence program can be used to read programs.

Using the Card to Expand the Data Memory Area

Data written to data registers and other destinations is written to the IC memory card. When the card is used in this way, the IC memory card can be used as an expanded memory area that lets data be written and read using the sequence program.

Data is written using the **F13 (ICWT)** instruction of the sequence program, and is read from the IC memory card using the **F12 (ICRD)** instruction.
The FROM type of card can only be used for reading data.

How the IC memory card is used



7.2 Formatting and Erasing

7.2.1 Program Memory Field and Expanded Memory Field

The area in which sequence programs are stored is called the “program field”, and the area used to expand the data memory is called the “expanded memory field”. The IC memory card must be divided into separate fields, depending on how it is being used.

Using the Card Only as a Program Memory

When using the card only to save programs, the entire IC memory card must be designated as a “program memory field”.

FROM type

Procedure:

1. **On the “Tool” menu, choose “IC Card Service” and then “Erase IC Card...” to erase the entire field.**
2. **On the “Tool” menu, select “IC Card Service” and then “Copy File to IC Card...” and set the format size to the maximum size. Then copy the program from a floppy disk or the hard disk, to the IC memory card.**

SRAM type

Procedure:

On the “Tool” menu, choose “IC Card Service” and then “Format IC Card...” to format the entire field.

Using the Card Only as a Data Memory Area

When using the card only to expand the data memory area, the entire IC memory card must be designated as an “expanded memory field”.

FROM type

Procedure:

1. **On the “Tool” menu, choose “IC Card Service” and then “Erase IC Card...” to erase the entire field.**
2. **Using the “Data Editor” supplied with the FPWIN GR, run the “Download to PLC” function, and transfer the data.**

SRAM type

Procedure:

On the “Tool” menu, choose “IC Card Service” and then “Erase IC Card...” to erase the entire field.

Using Different Sections of the Card as a Program Memory Field and Expanded Memory Field

Any desired settings may be entered for the field to be formatted. Of the entire field, any part of the field not formatted (program memory field) is used to expand the memory field.

FROM type

Procedure:

1. **On the “Tool” menu, choose “IC Card Service” and then “Erase IC Card...” to erase the entire field.**
2. **On the “Tool” menu, select “IC Card Service” and then “Copy File to IC Card...” to specify the format size. Then copy the program from a floppy disk or the hard disk, to the IC memory card.**
3. **Boot the “Data Editor”.**
4. **In the “Edit IC Memory Card Data” mode, create a file, or open an existing file.**
5. **On the “File” menu, select “Download to PLC”, and transfer the data.**

SRAM type

Procedure:

On the “Tool” menu, choose “IC Card Service” and then “Format IC Card...”. Specify the necessary segment as a program memory, and format it.

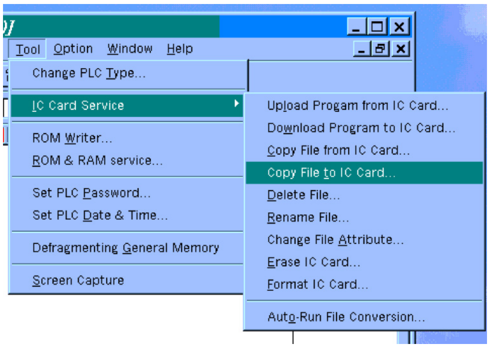
7.2.2 Procedure for Formatting the IC Memory Card

Formatting an FROM type

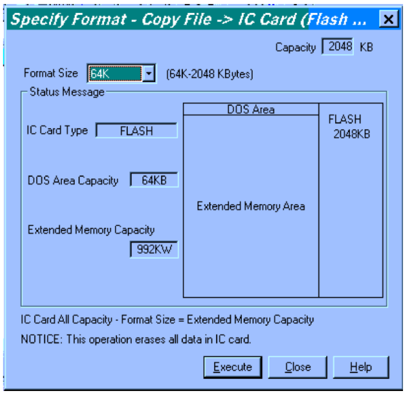
When using this type, formatting is done at the same time that the program on the disk is copied to the IC memory card, with the FPWIN GR.

Procedure:

1. **Boot the “Copy File to IC Card...” function.**



On the “Tool” menu, select “IC Card Service” and then “Copy File to IC Card...”. First, the “Specify Format” window opens.



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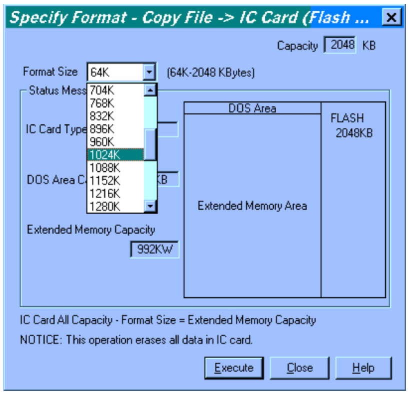
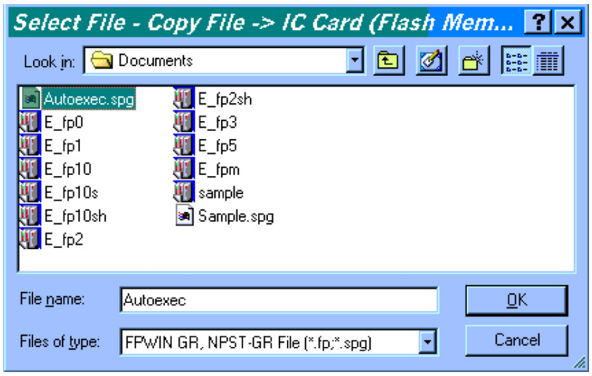
2. Specifying and running the format size

Press the button next to “Format Size” to select the size.



Next, click on the “Execute” button to open the “Select File” window.



3. Selecting the file to be copied

Select the file to be copied to the IC memory card, and click on “OK”.

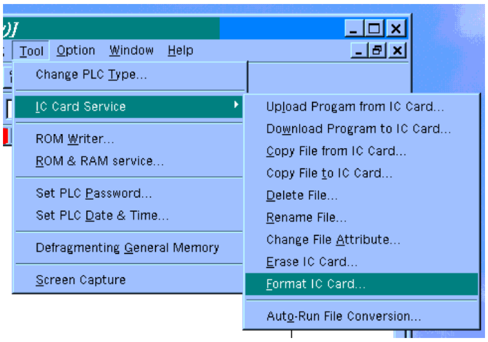
The IC memory card is formatted, and the file is written to the card.

Formatting the SRAM type

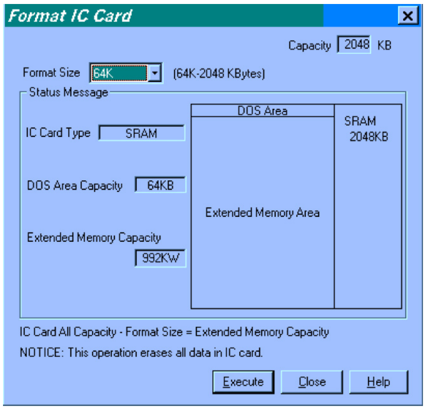
With this type of card, the IC memory card must be formatted before the program is saved to it, and a “program memory field” must be assured to which the program will be saved. This section explains how this is done using the FPWIN GR.

Procedure:

1. Booting the “Format IC Card...” function.



On the “Tool” menu, select “IC Card Service” and then “Format IC Card...”. The “Format IC Card” window opens.



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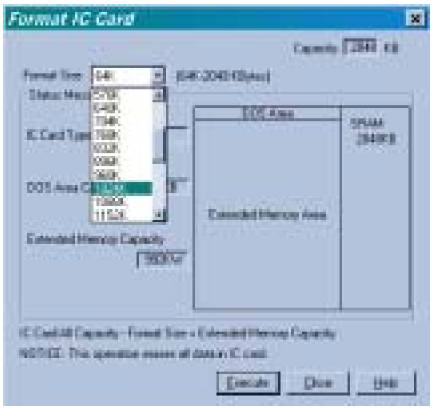
2. **Specifying and running the format size**
Press the ▼ button next to “Format Size” to select the size.



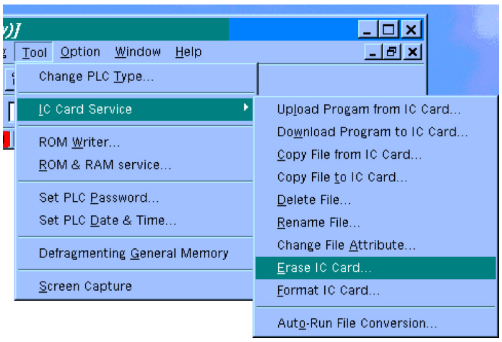
Next, click on the “Execute” button to format the card at the specified size.

7.2.3 Procedure for Erasing the IC Memory Card

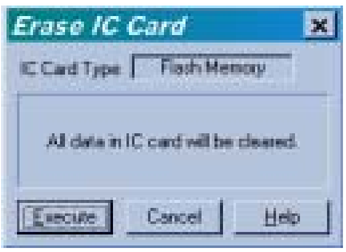
For both the SRAM type and the FROM type, before the IC memory card can be used as an expanded memory, any data already on the card must be erased, and an area must be assured as the “expanded memory field”. The procedure is described here using the FPWIN GR.

Procedure:

1. **Booting the “Erase IC Card...” function**



On the “Tool” menu, select “IC Card Service” and then “Erase IC Card...”. The “Erase IC Card” window opens.



2. **Erasing the card**
   Clicking on the “Execute” button starts erasing the data from the card. It takes approximately 1 minute to erase all the data.

   ***Once erasing the data starts, the “IC memory card access LED” on the CPU unit lights up.**
   The LED is turned off on completion of erasing.

7.2.4 Data Storage Capacity of IC Memory Card

When storing a program or data in the IC memory card, the data storage capacity is as follows.

	Program file (*.fp, *.SPG)
+	FAT area (see note)
	Total number of bytes

Keep the total number of bytes for the files given above less than the format capacity.

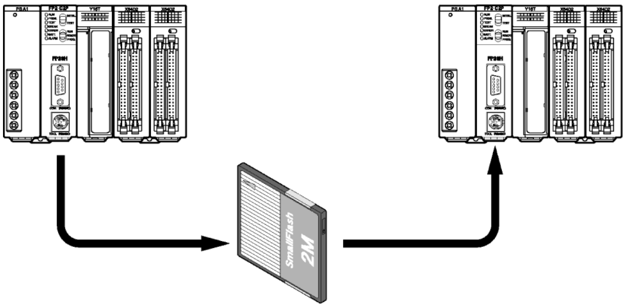
Note

The I/O comment capacity changes according to the size of the statements.
FAT area:
256KB format = 5.5KB
512KB format = 6KB
1MB format = 9.5KB
2MB format = 14.5KB

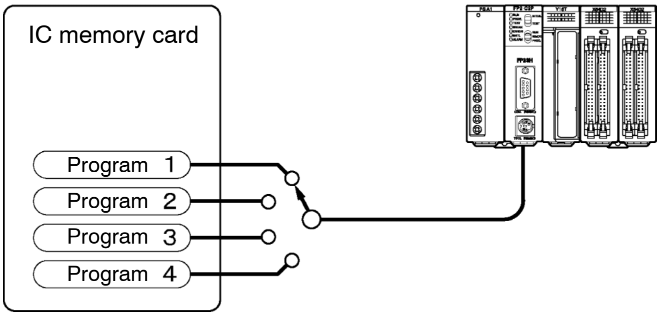
7.3 For Use as Program Memory

7.3.1 Writing the Program

By saving the program to the IC memory card, it is simple to create a backup or transfer it to another CPU.



Furthermore, by saving more than one program, switching between the programs can be done as necessary.



Writing Programs

There are three ways to write programs to the IC memory card:

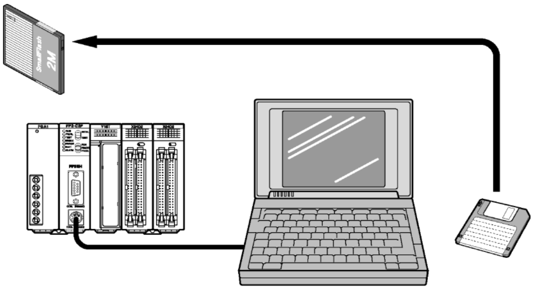
Use the “Copy File to IC Card...” function in the FPWIN GR to write a program saved on a disk directly to the IC memory card. All types of cards can be used for this.

Write programs created with the FPWIN GR directly to the IC memory card. This can only be done with SRAM types. (*)

Write programs in the RAM of the CPU to the IC memory card. This can only be done with SRAM types. (*)

*When writing programs to the FROM type of card, the program should be saved to a disk before using the “Copy File to IC Card...” function of the FPWIN GR to write the program to the IC memory card.

Method 1: Use the “Copy File to IC Card...” function in the FPWIN GR, directly write the program that is saved on the disk to the IC memory card. (For all types of IC memory card)



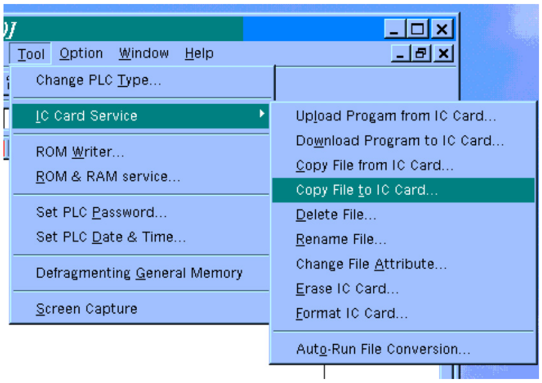
Procedure:

For FROM types

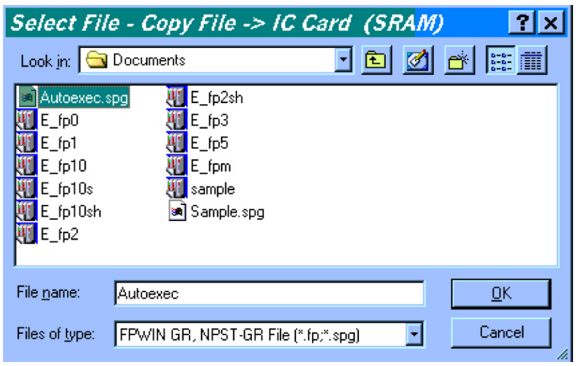
See section 7.2.2, “Procedure for Formatting the IC Memory Card”.

For SRAM types

1. **Boot the “Copy File to IC Card...” function.**
   On the “Tool” menu, select “IC Card Service” and then “Copy File to IC Card...”.



The “Select File” window opens.



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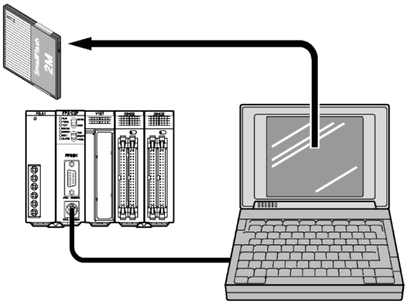
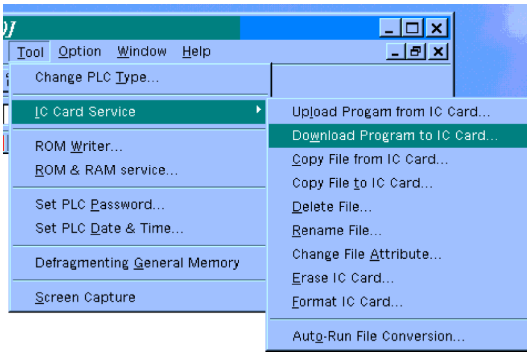
2. Selecting the file to be copied
Select the file to be copied to the IC memory card, and click on “OK”.
Writing of the file to the IC memory card begins, and the “List of File Copy Results” is displayed.

Method 2: Directly write the program that is made by the FPWIN GR to the IC memory card. (For the SRAM type IC memory card)

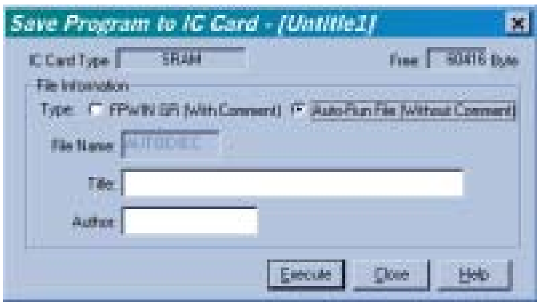


Procedure:

1. Booting the “Download Program to IC Card...” function
On the “Tool” menu, select “IC Card Service” and then “Download Program to IC Card...”.



The “Save Program to IC Card” window opens.

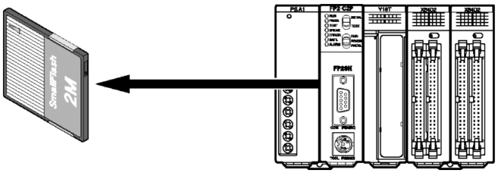


2. Setting the file information
Enter the “File Name” (name of the file to which the program is to be written), the “Title”, and the “Author” (name of the person creating the file).
The file name must be within 8 characters.
Programs can be written even if the “Title” and the “Author” are not specified.
Check to make sure the necessary items have been entered, and click on the “Execute” button.
Writing of the program to the IC memory card begins.

☞ Note

To have the program being sent executed automatically, select “Auto–Run File (Without Comment)” for the “Type” of “File Information”.

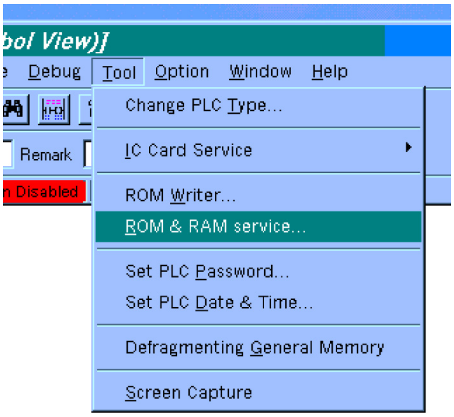
Method 3: Write a program on the RAM of the CPU into the IC memory card. (For the SRAM type IC memory card)



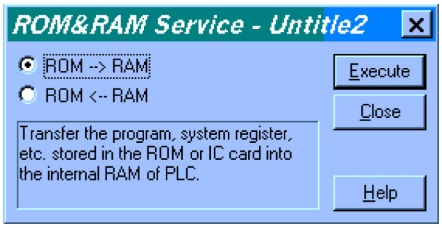
By performing the following procedures, the data on the RAM of the CPU is written to the IC memory card and named “Autoexec.spg”.

Procedure:

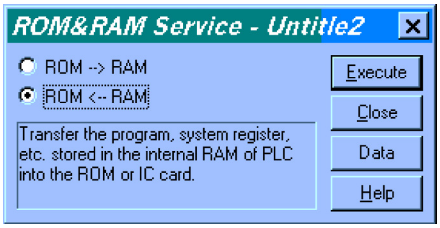
1. **Booting the “<u>R</u>OM & RAM service...” function**
   On the “<u>T</u>ool” menu, select “<u>R</u>OM & RAM service...”.



The “ROM & RAM Service” window opens.



2. **Executing the “ROM ← RAM” transfer function**
   Select “ROM ← RAM”, and click on the “<u>E</u>xecute” button.



7.3.2 Reading the Program

There are four methods of reading the program saved in the IC memory card.

Read the program on the IC memory card and directly transfer it into the internal RAM of the CPU at the same time that the power is turned on.

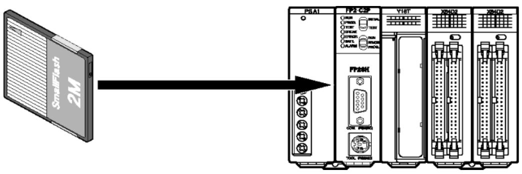
Use the programming tool to read the program of the IC memory card and directly transfer it into the internal RAM of the CPU.

Use the “Copy File from IC Card...” of the FPWIN GR, and select one of the programs saved in the IC memory card and read it to the FPWIN GR (memory of personal computer).

Use the **F14 (PGRD)** instruction to read the program from the IC memory card, and directly transfer it into the internal RAM of the CPU.

Method 1: Read the program on the IC memory card and directly transfer it into the internal RAM of the CPU at the same time that the power is turned on.

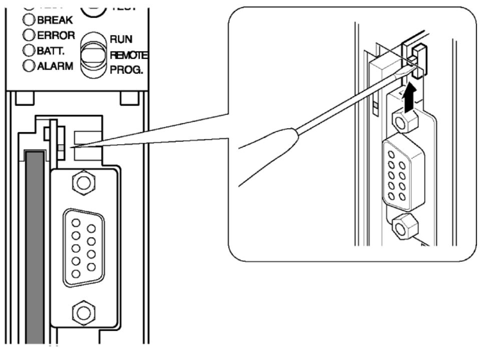
By just turning on the power of CPU, the device automatically reads the program of the IC memory card and transfers the program to the internal RAM of the CPU.



The target of automatic reading is the program named “Autoexec.spg”.

Procedure:

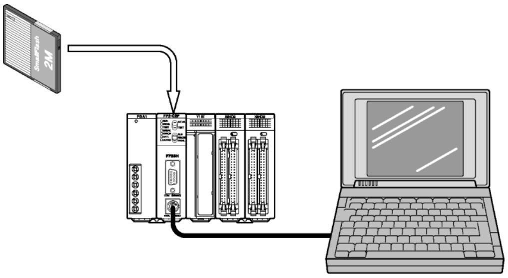
1. **While the power is turned off, set the DIP switches SW2 and SW4 on the back of the CPU to on, and set the IC memory card access enable switch to on position.**



2. **Turn on the CPU.**

Method 2: Use the programming tool to read the program of the IC memory card and directly transfer it into the internal RAM of the CPU.

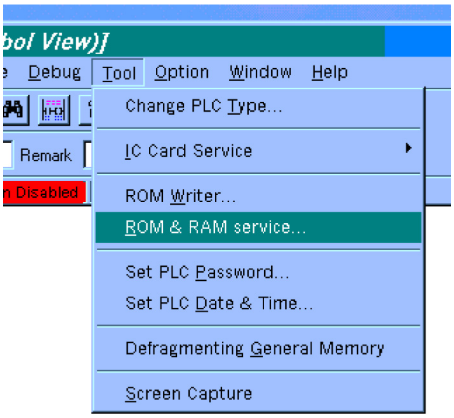
With simple operation of the programming tool, reads the program saved on the IC memory card, and transfer it to the internal RAM of the CPU.



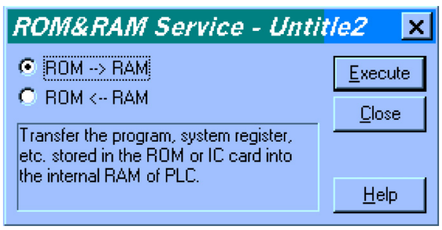
The target of automatic reading is the program named “Autoexec.spg”.

Procedure:

1. Booting the “ROM & RAM service...” function
On the “Tool” menu, select “ROM & RAM service...”

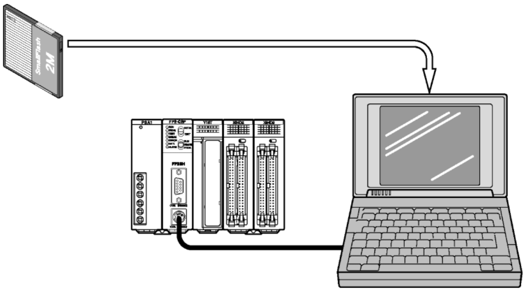


The “ROM & RAM Service” window opens.



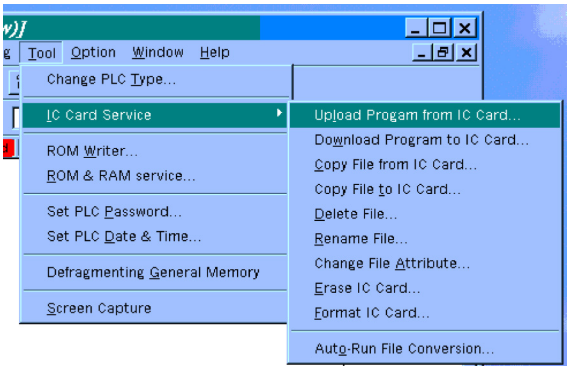
2. Executing the “ROM → RAM” transfer function
Select “ROM → RAM”, and click on the “Execute” button.

Method 3: Use the “Upload Program from IC Card...” of the FPWIN GR, and select one of the programs saved in the IC memory card and read it to the FPWIN GR (memory of personal computer).

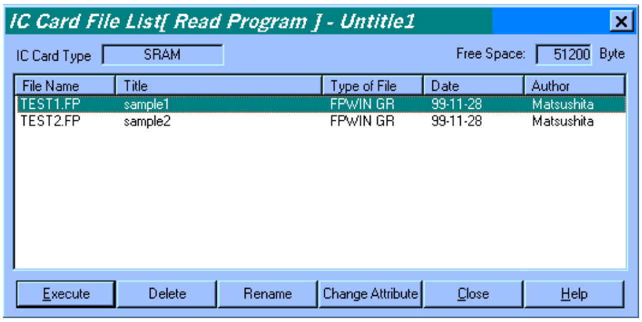


Procedure:

1. **Booting the “Upload Program from IC Card...” function**
   On the “Tool” menu, select “IC Card Service” and then “Upload Program from IC Card...”.

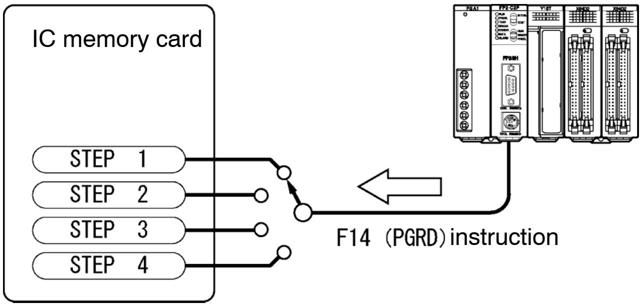


The “IC Card File List” is displayed.



2. **Selecting the file to be read**
   Select the file to be read from the “IC Card File List”, and click on the “Execute” button. Reading of the program begins.

Method 4: Use the **F14 (PGRD)** instruction to read the program from the IC memory card and directly transfer it into the internal RAM of the CPU.

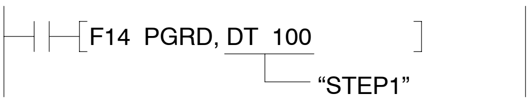


By first saving the programs you desire on the IC memory card, you can use the **F14 (PGRD)** instruction in the program, to switch a program while in the RUN mode (while in operation).

The following details the describe the program after executing **F14 (PGRD)** instruction.
The program will continue executing until the **END** instruction is executed.
The CPU enters the PROG. mode and the program is read from the IC memory card and transfer to the internal RAM of the CPU.
The CPU automatically switches to the RUN mode, and the new program executes.

Example:

With F14 (PGRD) instruction, specify a saved file name by the FPWIN GR to call up the program of from IC memory card.



For the program above, the contents "STEP 1" stored in DT100 is the file name used to call up the program.

To store the program name to registers such as DT100, you can write it with alphanumeric code using **F0 (MV)** or **F1 (DMV)** instruction, or you can write it with ASCII conversion using **F95 (ASC)** instruction. For more details, refer to the programming manual.

Notes

- **There are dangers involved when switching programs while in the RUN mode. Carefully read the section regarding the F14 (PGRD) instruction in the programming manual.**
- **Only files saved with the .spg extension are programs that can be read using the F14 (PGRD) instruction.**

7.4 For Use as Expansion Memory

Outline of Expansion Memory

The expansion memory area is an independent area from the internal memory of the CPU that stores word data. Use the **F12 (ICRD)** and **F13 (ICWT)** instructions to read and write data to this area. Below are some of the things that you can do by using the expansion memory area.

1) As reading and writing are easily done using high−level instructions, you can use the expansion memory as external memory for the CPU.

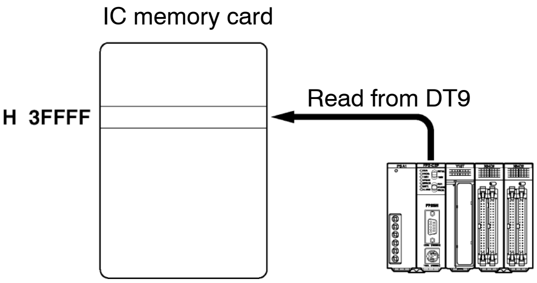
Writing (for SRAM type)

Use the **F13 (ICWT)** instruction to transfer the word data stored in the data register of the CPU to the IC memory card.

```
|—| |—[F0  MV , K  100 , DT 9 ]
       [F13  ICWT , DT  9 , K 1 , H3FFFF ]
```

With the above program, after the constant K100 is stored in DT9, **F13 (ICWT)** instruction is used to write one word of data (K100) from the beginning of DT9 to the address H3FFFF of the IC memory card. For more details, refer to the programming manual.

With the FROM type, the “Data Editor” is used to write programs.

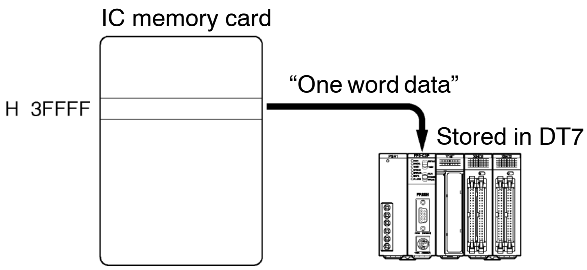


Reading

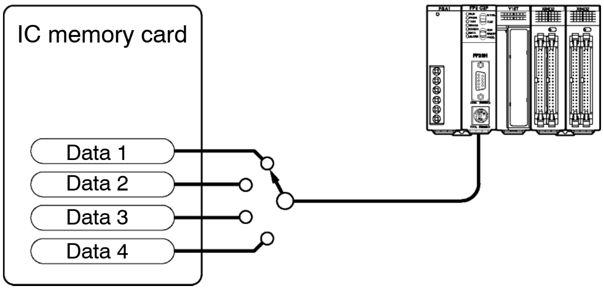
Use the **F12 (ICRD)** instruction to transfer the word data stored on the IC memory card to the data register of the CPU.

```
|—| |—[F12  ICRD , H3FFFF , K 1 , DT 7 ]
```

The above program reads a one word data from the address H3FFFF of the IC memory card to DT7. For more details, refer to the programming manual.



2) When dealing with many different data or other such applications, you can create a table to store the different control data and easily switch between the data ac– cording to the data type you are using.



Create a data table in the IC memory card such as outlined above, so that the data is read to the CPU every time you switch data.

When using the IC memory card as an expanded memory, the DIP switches do not need to be set, but the access enable switch should be set to “on”.

Configuration of Expanded Memory Field

Fields of the IC memory card that are not formatted can be used as expanded memory field.

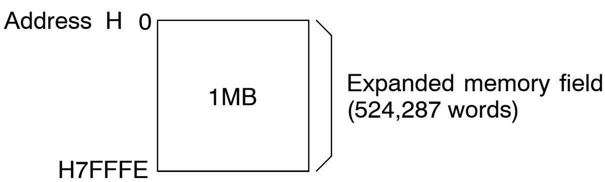
1) Using the entire IC memory card as expansion memory (when there is no DOS formatted field) The “Card capacity – 1” word portion can be used.

The data of one word (two bytes) can be stored in one address. As the following example calculation, in 2MB area, data of 1,048,575 words can be stored.

$$\frac{(2 \times 1048576)\text{ bytes}}{2} - 1 = 1{,}048{,}575 \text{ words}$$

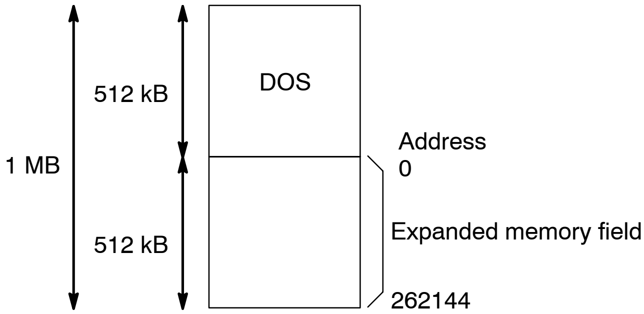
In the expanded memory field, the addresses are numbered by word units and, regardless of the size of the formatted area, the starting address is numbered as 0 (H0). For example, the addresses for 1MB (512k words) area are from as H0 to H7FFFE.

Example: When 1MB of SRAM type IC memory card is designated as expansion memory.



2) Using the remaining DOS formatted field
All of the remaining DOS formatted field can be used as expansion memory.

Example: When 512 kB is set as the DOS formatted field in a 1 MB card



7.5 Menus Related to Tool Software

The FPWIN GR is equipped with menus that are used for management of the IC memory card.

Reading Programs and Data Stored on IC Memory Cards

"Upload Program from IC Card..."

This enables one program to be selected from among the multiple programs stored on the IC memory card, and read to the FPWIN GR.

"Copy File from IC Card..."

This reads a program or data file stored on the IC memory card, and copies it to a floppy disk (or hard disk).
When creating a copy of a file stored on the IC memory card, first copy the file stored on the IC memory card, that serves as the source file, using this menu, and then insert the new IC memory card and use "Copy File from IC Card..." to copy the data from the disk to the IC memory card.

Initializing the IC Memory Card

"Erase IC Card..."

This clears all of the contents from the IC memory card. The program field assured with the "Format IC Card..." function is cleared, and the entire card is used as an expanded memory field.

Management of an SRAM type of IC Memory Card

Before using the card

"Format IC Card..."

The IC memory card is formatted, and a "program memory field" is assured in which programs can be saved. The remaining area assured as the "program memory field" then serves as an expanded memory area.

Writing data to the IC memory card

"Download Program to IC Card..."

Programs are written from the FPWIN GR to the IC memory card.

"Copy File to IC Card..."

The contents of a floppy disk (or hard disk) are copied to the IC memory card. This function can also be used to select multiple programs and write them to the IC memory card as a batch, all at once.

Other file management menus

"Delete File..."

This deletes programs from the IC memory card. This function can also be used to select multiple programs and delete them as a batch, all at once.

"Rename File..."

This is used to change the file name or title of a program on the IC memory card.

"Change File Attribute..."

This is used for dedicated reading of programs stored on the IC memory card, or to change the attributes of a hidden file.

Writing to an FROM Type IC Memory Card

"Copy File to IC Card..."

Programs are written to an FROM type of IC memory card by copying the contents of a floppy disk (or hard disk) to the card.

With the FROM type of IC memory card, it is not possible to update only partial sections of data, or to change file names or delete files. These functions should be carried out on the disk before the data is copied to the IC memory card.

Chapter 8

Self-Diagnostic Function and Troubleshooting

8.1 Self-Diagnostic Function

8.1.1 LED Display for Status Condition

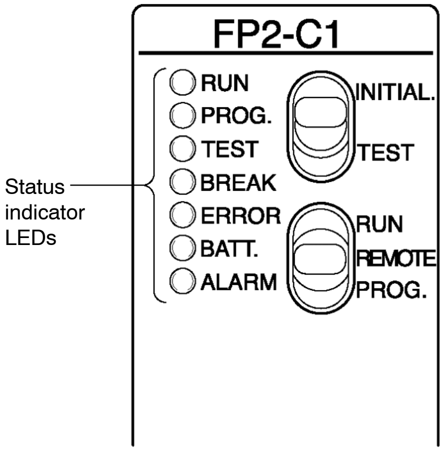
Status Indicator LEDs on CPU

Condition	LED status							Description	Operation (Program execution) status
	RUN	PROG.	TEST	BREAK	ERROR	BATT.	ALARM		
Normal condition	on	off	off	off	off	off	off	Normal operation	Operation
	off	on	Varies	off	off	off	off	PROG. mode	Stop
	Flashes	off	Varies	off	off	off	off	Forcing on/off in RUN mode	Operation
	off	on	on	Varies	Varies	off	off	TEST operation mode (break condition)	Stop
	on	off	on	off	Varies	off	off	TEST operation mode (operating condition)	Operation
Abnormal condition	off	on	Varies	Varies	on	Varies	off	When a self-diagnostic error occurs (break condition)	Stop
	on	off	off	off	on	Varies	off	When a self-diagnostic error occurs (operating condition)	Operation
	Varies	Varies	Varies	Varies	on	on	off	When CPU backup battery error occurs	Operation
	Varies	Varies	Varies	Varies	Varies	Varies	on	When a watchdog timer error occurs	Stop
	off	Flashes	Varies	off	Varies	Varies	off	When remote I/O slave station waiting error occurs	Stop

Status Indicator of CPU

The CPU has a self-diagnostic function which identifies errors and stops operation if necessary.

When an error occurs, the status of the status indicator LEDs on the CPU vary, as shown in the table above.



8.1.2 Operation When an Error Occurs

Normally, if an error occurs, the operation stops.

There are some instances in which operation continues even if an error occurs, such as with a battery error.

The user may select whether operation is to be continued or stopped if a duplicated output error or operation error occurs, by setting the system registers. You can set the system registers for error which operation is to be continued or stopped using programming tool software (NPST−GR/FPWIN GR).

PLC Configuration (System register) Setting Menu of FPWIN GR Software

1. **On the “Option” menu, select “PLC Configuration”.**
2. **In the [PLC Configuration] Screen, select [Action on Error] tab.**

Register No.	Item	Description
20	DUPLICATE OUTPUT	[DISE, ENAB]
21	I/O UNIT ERROR	[STOP, CONT]
22	INTELLIGENT UNIT ERROR	[STOP, CONT]
23	I/O VERIFY ERROR	[STOP, CONT]
24	UNUSED	
25	UNUSED	
26	OPERATION ERROR	[STOP, CONT]
27	REMOTE I/O SLAVE LINK ERROR	[STOP, CONT]
28	I/O ERROR IN REMOTE I/O SLAVE	[STOP, CONT]
29	UNUSED	
4	BATTERY ERROR INDICATION	[ENAB, DISA]
	INDEX MODIFIER CHECK	[ENAB, DISA]

Allowing duplicated output

When you set the system register 20 to “ENAB”, duplicated output is not regarded as an error and the PLC continues to operate.

Continuing after an operation error

When you set the system register 26 to “CONT”, even if the PLC continues to operate, this is regarded as an error.
This applies to system registers 21 through 28 as well.

8.2 Troubleshooting

8.2.1 If the ERROR LED Lights

Condition

The self-diagnostic error occurs.

Procedure 1

Replace the backup battery of the CPU when the BATT. LED is on. (☛ section 9.1.1)

Procedure 2

Check the error code using the programming tool.

Using programming tool software (FPWIN GR)
In the ONLINE mode, select “Status Display” on the “Online” menu. At the bottom of the “STATUS DISPLAY” window, you can find the error code.

SLF DIAGN ERR CD $\underbrace{\text{(45)}}_{\text{Error code}}$ $\underbrace{\text{[OPERATION ERROR]}}_{\text{Comments}}$

Procedure 3

Error code is 1 to 9

Condition

There is a syntax error in the program.

Operation 1

Change to PROG. mode and clear the error.

Operation 2

Execute a total−check function using programming tool software (FPWIN GR) to determine the location of the syntax error.

☛ next page

Error code is 20 or higher

Condition

A self-diagnostic error other than a syntax error has occurred.

Operation

Use the programming tool in PROG. mode to clear the error.

Using programming tool software (FPWIN GR)

Click “Clear Error” button in the “Status Display” menu described on the previous page. Error code 43 and higher can be cleared.

In the PROG. mode, the power supply can be turned off and then on again to clear the error, but all of the contents of the operation memory except hold type data are cleared.

An error can also be cleared by executing a self-diagnostic error set instruction **F148 (ERR)**/**P148 (PERR)**.

When an operation error (error code 45) occurs, the address at which the error occurred is stored in special data registers DT90017 and DT90018. If this happens, monitor the address at which the error occurred before cancelling the error.

8.2.2 If the ALARM LED Lights

Condition

The system watchdog timer has been activated and the operation of PLC has been stopped.

Procedure 1

Set the mode selector of CPU from RUN to PROG. mode and turn the power off and then on.

If the RUN and ALARM LED is turned on again, there is probably an abnormality in the CPU. Please contact your dealer.

If the ERROR LED is turned on, go to section 8.2.1.

Procedure 2

Set the mode selector from PROG. to RUN mode.

If the ALARM LED is turned on, the program execution time is too long. Check the program, referring the following:

Check if instructions such as **JP** or **LOOP** are programmed in such a way that a scan can never finish.

Check that interrupt instructions are executed in succession.

Procedure 3

If there is nothing wrong with programs, there may be a problem with the ambient environment.

Check the wirings including the grounding link.

Especially, check if the RS232C wiring is not close to power lines and it has been shielded.

8.2.3 If the LED (POWER) of the Power Supply Unit Does Not Light

Procedure 1

Check wiring of power supply unit.

Procedure 2

Check if the output of the power supply unit is in the range of the rating.

If the capacity of internally supplied power "5V" is insufficient, investigate different unit combinations.

Procedure 3

Disconnect the power supply wiring to the other devices if the power supplied to the power supply unit is shared with them.

If the LED on the power supply unit turn on at this moment, prepare another power supply for other devices.

8.2.4 If Outputting Does Not Occur as Desired

Proceed from the check of the output side to the check of the input side.

Check of output condition 1

Output indicator LEDs are on

Procedure 1

Check the wiring of the loads.

Procedure 2

Check if the power is properly supplied to the loads.

If the power is properly supplied to the load, there is probably an abnormality in the load. Check the load again.

If the power is not supplied to the load, there is probably an abnormality in the output section. Please contact your dealer.

Check of output condition 2

Output indicator LEDs are off

Procedure 1

Monitor the output condition using a programming tool.
If the output monitored is turned on, there is probably a duplicated output error.

Procedure 2

Forcing on the output using forcing I/O function.

If the output indicator LED is turned on, go to input condition check.

If the output indicator LED remains off, there is probably an abnormality in the output unit. Please contact your dealer.

Check of input condition 1

Input indicator LEDs are off

Procedure 1

Check the wiring of the input devices.

Procedure 2

Check that the power is properly supplied to the input terminals.

If the power is properly supplied to the input terminal, there is probably an abnormality in the input unit. Please contact your dealer.

If the power is not properly supplied to the input terminal, there is probably an abnormality in the input device or input power supply. Check the input device and input power supply.

Check of input condition 2

Input indicator LEDs are on

Procedure

Monitor the input condition using a programming tool.

If the input monitored is off, there is probably an abnormality with the input unit. Please contact your dealer.

If the input monitored is on, check the leakage current at the input devices (e.g., two-wire type sensor) and check the program again, referring the following:
Check for the duplicated use of output and for the output using the high−level instruction.
Check the program flow when a control instruction such as **MC** or **JP** is used.
Check the settings of the I/O allocation.

8.2.5 If a Communication Error Message Appears

Procedure 1

Make sure the computer and PLC are properly connected.

Procedure 2

Check if the baud rate and data length settings of the PLC and the computer are the same.

Personal computer section setting

1. On the “Option” menu, select “Communication Settings”.
2. Select a baud rate “9600 or 19200”.

PLC section setting

Use the SW1 of DIP switches (operation condition switches) to enter the setting for the PLC.
The SW1 “off” position is the system register setting.

Depending on the personal computer, there are times when baud rate of 19,200bps or greater are not supported. If problems occur, set both the personal computer and PLC to 9,600bps. If SW1 is on, the baud rate for the FP2/FP2SH PLC is fixed to 9,600bps.

8.2.6 If a Protect Error Message Appears

When Optional User ROM is Installed in the CPU

The program of the internal RAM cannot be modified using the programming tool and a “protect error” occurs.

Operation 1

Turn off the power supply of the PLC, remove the CPU and set the SW2 of DIP switches (operation condition switches) on CPU to the “off (internal RAM)” position.

Operation 2

Modify the program of the internal RAM using the programming tool.

Operation 3

Save the modified program to the memory or master memory and start operation again.

If the Program Memory is Protected

Operation

Turn off the power of the PLC, remove the CPU and set the SW3 of DIP switches (operation condition switches) on CPU to “off (write enabled)” position.

When a Password Function is Used

Operation

1. On the “Online” menu, select “Online Edit Mode”.
2. On the “Tool” menu, select “Set PLC Password”.
3. Enter the password and select “unprotect”.

Chapter 9

Maintenance

9.1 Replacement of Spare Parts

9.1.1 Backup Battery

Lifetime of Backup Battery

The life of the backup battery will eventually expire and therefore it is important to replace it with a new battery periodically. The battery lifetime will differ depending on the operating conditions (i.e., ambient temperature) and the type of expansion memory unit. Refer to the table below for a guide as to when to replace the battery.

Expansion memory unit type installed	Battery lifetime (ambient temperature: 55°C/131°F)
No expansion memory unit	For FP2: 10,000 hours or more (typical lifetime in actual use: approx. 13,000 hours) For FP2SH: 3,500 hours or more (typical lifetime in actual use: approx. 31,000 hours)
FP2–EM1 (Model No. AFP2201)	For FP2: 9,000 hours or more (typical lifetime in actual use: approx. 12,000 hours)
FP2–EM2 (Model No. AFP2202) **FP2–EM3 (Model No. AFP2203)**	For FP2: 8,000 hours or more (typical lifetime in actual use: approx. 12,000 hours)
FP2–EM6 (Model No. AFP2206)	For FP2: 8,500 hours or more (typical lifetime in actual use: approx. 12,500 hours)
FP2–EM7 (Model No. AFP2209)	For FP2: 10,000 hours or more (typical lifetime in actual use: approx. 13,000 hours) For FP2SH: 3,500 hours or more (typical lifetime in actual use: approx. 31,000 hours)
Model No. AFP2208	For FP2SH: 3,500 hours or more (typical lifetime in actual use: approx. 31,000 hours)

A drop in the battery voltage can be confirmed with special internal relays R9005 and R9006, the ERROR LED and BATT. LED. Be sure to replace new battery within a week.

IC memory card	Battery lifetime (Ambient temperature of 25 °C)
	FP2SH
AFP2209	Approx 3 years or more

The battery voltage of IC card is detected only once when the CPU unit is powered on. An error will not be determined if the battery is replaced during power–on.
If the battery voltage has dropped, the ERROR LED lights, R9101 or R9102 on, and error code K55 or K54 is stored in special data register DT90000. Error codes can be confirmed using programming tools.

Backup battery

PLC Type	Part number	Description	
FP2 CPU unit	AFC8801	Lithium battery CR2450 or equivalent	———
FP2SH CPU unit	AFP8801	———	Common to FP3 and FP10SH
IC memory card	AFP2806	———	BR–1225A/B

Notes

- **During RAM operation, save the program in the CPU onto disk using programming tool software (FPWIN GR).**
- **Never throw batteries into a fire, disassemble or charge the battery in order to prevent accidents such as bursting, fire or heat generation.**

Replacement Method of Backup Battery

Preparation

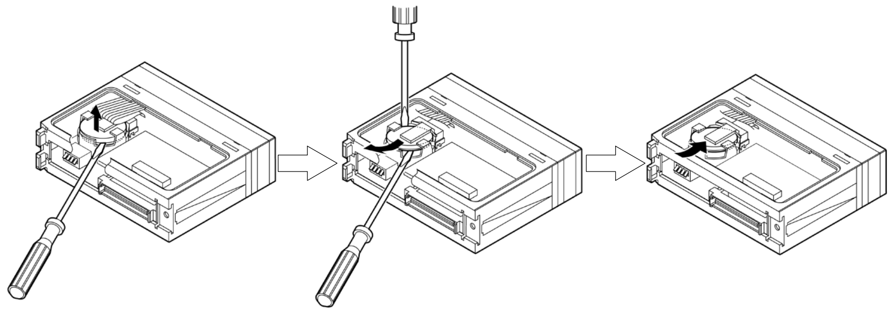
Leave the unit on for more than 30 minutes, then turn the power off and remove the CPU. It is recommended to save the programs and data within the CPU in a PC in case that it requires time for the replacement.

Note

After turning the power off, be sure to finish replacing the battery within 10 minutes.

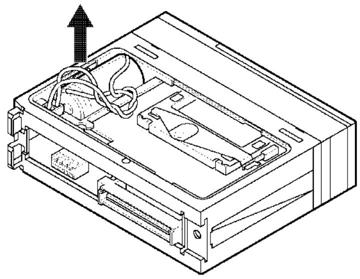
Procedure for FP2

1. **Use an insulated flat-head screwdriver and lift up the battery. During this operation, be careful not to damage printed circuit board, battery holder, or other internal components.**
2. **Pull out the battery in the direction shown by the arrows below (pushing from the rear).**
3. **Holding the positive pole of the battery upwards, press the new battery into the battery holder underneath the (+) terminal.**



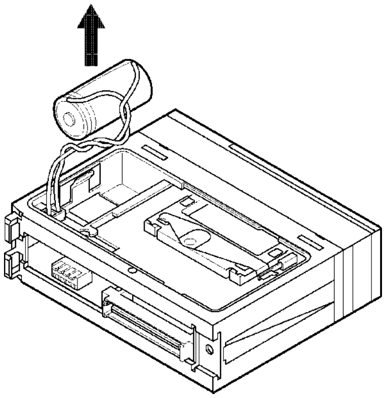
Procedure for FP2SH

1. **Lift up the lead wire.**

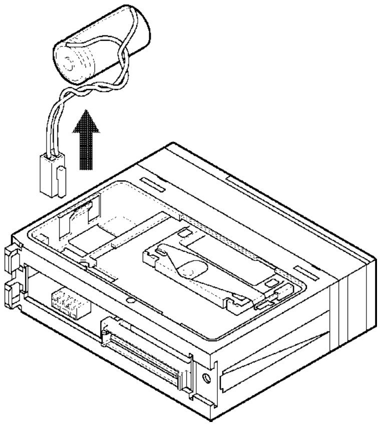


Make sure the lead wire next to the connector insertion area, which is also the battery holder, is lifted out of the hole that secures it in place.

2. **Lift up the battery.**



3. **Pull the connector off.**



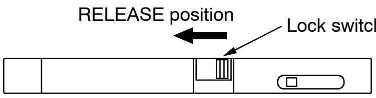
Pull the connector straight off, so the terminals do not bend.

4. **Install the new battery by reversing the above procedure.
Make sure the connector terminals are positioned in the correct directions.**

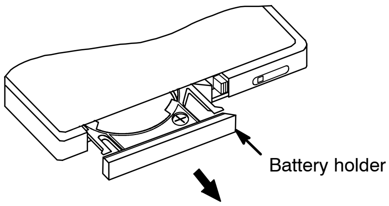
Procedure for AFP2209:

Preparation
Backup the data saved in the IC memory card.
Note: The saved data is overwritten when replacing the battery.

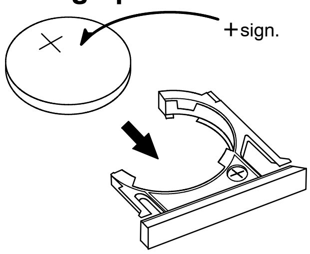
1. **Move to the lock switch to the RELEASE position (toward the battery holder).**



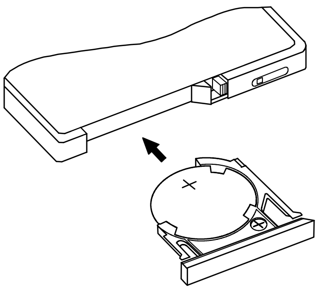
2. **Remove the battery holder.**



3. **Place the battery in the battery holder with the side with a '+' sign facing up.**



4. **Insert the battery holder with the battery all the way seated in the IC memory card.**
   *** The lock swich is automatically back to the LOCK position when removing the battery holder.**
   In this state, insert the battery holder all the way seated.



Confirm the lock switch is in the LOCK position.

5. **Write the backup data in the IC memory card.**

9.1.2 Removable Terminal Block for Input and Output Units

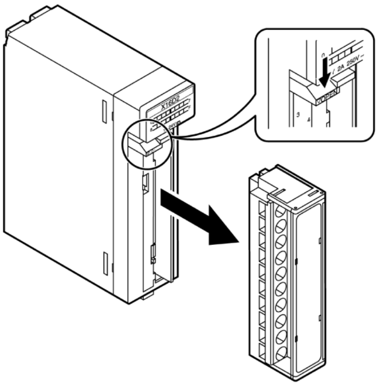
Removable Terminal Block

The removable terminal block is used on the terminal block type input and output units. The removable terminal block can be removed while it is still wired. Therefore, if a malfunction or other error occurs, replacement of the unit and other maintenance procedures can be carried out speedily.

Replacement of Removable Terminal Block

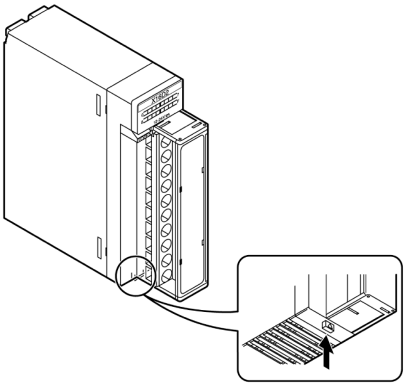
Removal procedure

The whole removable terminal block for terminal block type input and output units can be removed by lowering the “OPEN” knob (release lever) on the top of the terminal block. Used at the time of wiring.



Installation procedure

To replace the terminal block, press it into its original position until it is completely seated and press the terminal block lock button on the bottom of the unit to secure the terminal block in place. Then verify that the terminal block is properly secured and cannot be removed.



9.2 Preventive Maintenance

Although the FP2/FP2SH system has been designed in such a way to minimize maintenance and offer troublefree operation, several maintenance aspects should be taken into consideration.

If preventive maintenance is performed periodically, you will minimize the possibility of system malfunctions.

Inspection item	Inspection description	Basis of judgement	Reference
Power supply unit	Check POWER LED on power supply unit	Normal if on	Section 2.7
	Power supply unit	Periodic replacement (20,000 hours of operation)	
CPU display	Check RUN LED	On in RUN state	Section 2.2, 2.4, and 8.1
	Check ERROR LED	Normal if off	
	Check ALARM LED	Normal if off	
	Check BATT. LED	Normal if off	
Input/output unit display	Check input/output display LED	Normal if "light" during on, and "not light" during off	Section 2.8
Installation condition	Backplane mounting looseness	Securely mounted	Section 4.1.1 and 4.1.2
	Looseness and/or play in unit		
Connection condition	Looseness of terminal screw	No looseness	Section 4.1.3, 4.2, 4.4 and 4.5
	Proximity of connection in pinch terminal	Pinched parallel	
	Connector looseness	Locked in	
	Connection condition of expansion cable	Connector section is not loose	
Power supply voltage of power supply unit	Voltage between terminals	FP2−PSA1: 100 to 120V AC FP2−PSA2: 200 to 240V AC FP2−PSA3: 100 to 240V AC FP2−PSD2: 24V DC	Section 4.2.1
Power supply voltage for input/output	Voltage between terminals	Within the specified range of each unit	Section 2.9 to 2.11
Ambient environment	Ambient temperature	0 to 55°C/32 to 131°F	Section 4.1.1
	Ambient humidity	30 to 85% RH	
	Operating condition	No dust or corrosive gas	
Backup battery	Battery for CPU	Regular replacement	Section 9.1.1
	Battery for IC memory card		

Chapter 10

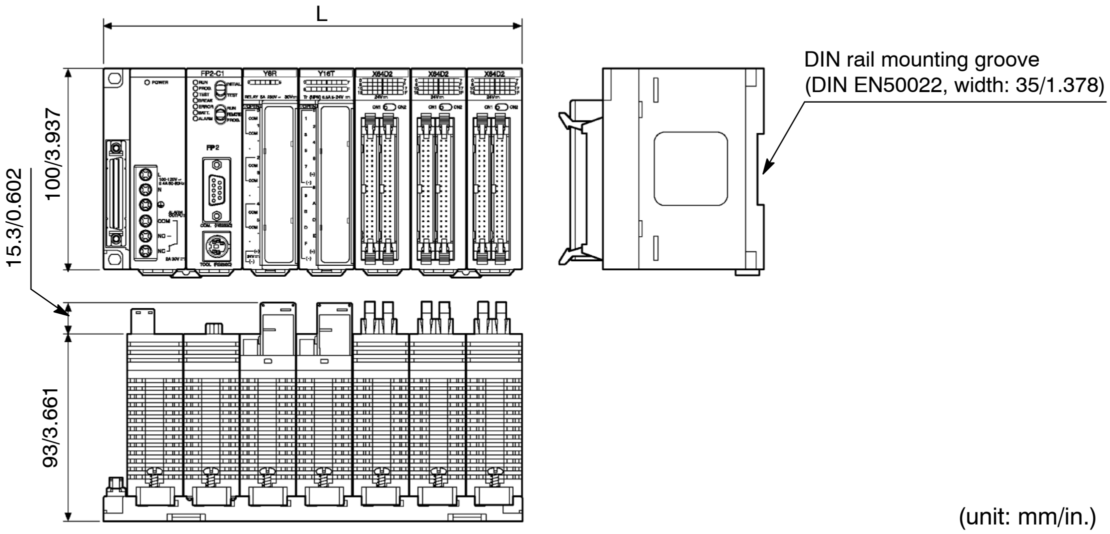
Specifications

10.1 Specifications

General Specifications

Item	Descriptions
Ambient temperature	0 to +55°C/32 to 131°F
Storage temperature	–20 to +70°C/–4 to +158°F
Ambient humidity	30 to 85% RH (at 25°C non-condensing)
Storage humidity	30 to 85% RH (at 25°C non-condensing)
Breakdown voltage	1,500V AC, 1 minute between AC external terminal and frame ground terminal
	500V AC, 1 minute between DC external terminal and frame ground terminal
Insulation resistance	100MΩ or more (measured with a 500V DC megger testing) between external terminal and frame ground terminal
Vibration resistance	10 to 55Hz, 1 cycle/min: double amplitude of 0.75mm/0.030 in., 10 min on 3 axes
Shock resistance	98m/s^2, 4 times on 3 axes
Noise immunity	1,500 Vp-p with pulse widths 50ns and 1μs (based on in-house measurements)
Operating conditions	Free from corrosive gases and excessive dust

Dimensions



(unit: mm/in.)

FP2 backplane

Item	Description				
Number of module	5 modules	7 modules	9 modules	12 modules	14 modules
L (mm/in.)	140/5.512	209/8.228	265/10.433	349/13.740	405/15.945

FP2 backplane H type

Item	Description	
Number of module	Basic backplane 11 modules	Expansion backplane 10 modules
L (mm/in.)	349/13.740	349/13.740

The illustration above shows the 7-module type. The 5-module type does not have an expansion connector.

Table of Weight

Type				Part number	Weight (Approx.)
FP2 CPU				FP2–C1	130g
				FP2–C1D	220g
				FP2–C1SL	250g
FP2SH CPU				FP2–C2L	130g
				FP2–C2	130g
				FP2–C2P	170g
				FP2–C3P	170g
Backplane				FP2–BP05	180g
				FP2–BP07	280g
				FP2–BP09	350g
				FP2–BP12	470g
				FP2–BP14	530g
				FP2–BP11MH	470g
				FP2–BP10EH	470g
FP2 Power supply unit				FP2–PSA1	180g
				FP2–PSA2	180g
				FP2–PSA3	280g
				FP2–PSD2	300g
Input unit	**DC input**	**16-point terminal type, 12 to 24V DC**		FP2–X16D2	140g
		32-point connector type, 24V DC		FP2–X32D2	100g
		64-point connector type, 24V DC		FP2–X64D2	120g
Output unit	**Relay output**	**6-point terminal type**		FP2–Y6R	170g
		16-point terminal type		FP2–Y16R	190g
	Transistor output	**16-point terminal NPN type**		FP2–Y16T	150g
		32-point connector NPN type		FP2–Y32T	100g
		64-point connector NPN type		FP2–Y64T	120g
		16-point terminal PNP type		FP2–Y16P	150g
		32-point connector PNP type		FP2–Y32P	100g
		64-point connector PNP type		FP2–Y64P	120g
I/O mixed unit	**32-point 24V DC input/32-point connector NPN output type**			FP2–XY64D2T, FP2–XY64D7T	120g
	32-point 24V DC input/32-point connector PNP output type			FP2–XY64D2P, FP2–XY64D7P	120g
Intelligent unit	**Analog input unit**			FP2–AD8VI, FP2–AD8X, FP2–RTD	160g
	Analog output unit			FP2–DA4	160g
	High–speed counter unit	**NPN**		FP2–HSCT	110g
		PNP		FP2–HSCP	
	Pulse I/O unit	**NPN**		FP2–PXYT	130g
		PNP		FP2–PXYP	
	Positioning unit	**2-axis type**		FP2–PP2	125g
		4-axis type		FP2–PP4	150g
	Positioning unit (Multifunction type)	**2-axis type**	**Transistor output type**	FP2–PP21	105g
			Line driver output type	FP2–PP22	
		4-axis type	**Transistor output type**	FP2–PP41	120g
			Line driver output type	FP2–PP42	
	Positioning unit (Interpolation type)	**2-axis type**	**Transistor output type**	FP2–PP2T	140g
			Line driver output type	FP2–PP2L	150g
		4-axis type	**Transistor output type**	FP2–PP4T	140g
			Line driver output type	FP2–PP4L	150g
	Serial data unit			FP2–SDU	120g
	Multi communication unit		**Main unit**	FP2–MCU	130g
			Communication block	FP2–CB232 FP2–CB422 FP2–CB485	35g
	Computer communication unit			FP2–CCU	120g

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Type				Part number	Weight (Approx.)
Intelligent unit	S-LINK unit			FP2–SL2	120g
	Multi-wire link unit			FP2–MW	110g
	ET–LAN unit, ET–LAN2 unit			FP2–ET1, FP2–ET2	125g
	MEWNET–VE link unit, MEWNET–VE2 link unit			FP2–VE, FP2–VE2	125g
	Remote I/O Slave Unit			FP2–RMS	110g
	FNS Unit	FNS Unit	Transistor output type	FP2–FNS	88g
		FP–FNS Block	PROFIBUS	AFPN–AB6200	31g
			Device Net	AFPN–AB6201	32g
			CAN open	AFPN–AB6218	32g
	FMU Unit		PROFIBUS	FP2–DPV1–M	118g
			Device Net	FP2–DEV–M	118g
			CAN open	FP2–CAN–M	118g
Expansion cable				FP2–EC	180g
				FP2–EC2	400g

FP2 Performance Specifications

Item		FP2 CPU
		FP2–C1 (AFP2211), FP2–C1D (AFP2212), FP2–C1SL (AFP2214)
Program/control method		Relay symbol/cyclic operation
Controllable I/O points	Basic construction	Using Backplanes: Max. 768 points (12 modules) Using Backplanes H type: Max. 512 points (8 modules)
	Expanded construction	Using Backplanes: Max. 1,600 points (25 modules) Using Backplanes H type: Max. 2,048 points (32 modules)
	Using remote I/O system	Max. 2,048 points (using S-LINK or MEWNET-F system)
Program capacity (* Note 1)	Internal memory	Approx. 16k steps
	Using expansion memory	Approx. 32k steps (* Note 2)
Number of instructions	Basic instructions	96 types
	High-level instructions	428 types
Operation speed (typical value)	Basic instructions	From 0.35μs per instruction
	High-level instructions	From 0.93μs per instruction
Operation memory points for relays	External input relays (X)	2,048 points (* Note 1)
	External output relays (Y)	2,048 points (* Note 1)
	Internal relays (R)	4,048 points (* Note 3)
	Timer/counter (T/C)	Total 1,024 points (* Note 3) – Timer: units of 1ms, 10ms, 100ms and 1s counts up to 32,767 × each unit – Counter: 1 to 32,767 counts
	Link relays (L)	2,048 points (* Notes 3 and 4)
	Pulse relays (P)	1,024 points (* Note 3)
	Alarm relays (E)	Not available
	Data registers (DT)	6,000 words (* Note 3)
	File registers (FL)	0 to 14,333 words (when expanding: 0 to 30,717 words) (* Note 3)
	Link data registers (LD)	256 words (* Notes 3 and 5)
	Timer/counter set value area (SV)	1,024 words
	Timer/counter elapsed value area (EV)	1,024 words
	Index registers (I0 to ID)	14 words

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10.1 Specifications

<table>
<tr><th rowspan="2">Item</th><th colspan="3">FP2 CPU</th></tr>
<tr><th colspan="3">FP2−C1 (AFP2211), FP2−C1D (AFP2212), FP2−C1SL (AFP2214)</th></tr>
<tr><td>Differential points</td><td colspan="3">Unlimited number of points</td></tr>
<tr><td>Auxiliary timer</td><td colspan="3">Unlimited number of points, down type timer (0.01 to 327.67s)</td></tr>
<tr><td>Shift register</td><td colspan="3">Max. 253 points</td></tr>
<tr><td>Master control relay points (MCR)</td><td colspan="3">256 points</td></tr>
<tr><td>Number of labels (JP and LOOP)</td><td colspan="3">256 points</td></tr>
<tr><td>Number of step ladder</td><td colspan="3">1,000 steps (* Note 3)</td></tr>
<tr><td>Number of subroutine</td><td colspan="3">100 subroutines</td></tr>
<tr><td>Number of interrupt program</td><td colspan="3">1 program (periodical interrupt: allows setting of the time interval within the range from 0.5ms to 1.5s)</td></tr>
<tr><td>Comment input function</td><td colspan="3">Available (* Note 6)</td></tr>
<tr><td>Sampling trace function</td><td colspan="3">Max. 1,000 samples (4,000 words) for 16 contacts and 3 words (* Note 2)</td></tr>
<tr><td>Clock/calendar function</td><td colspan="3">Available (year, month, day, hour, minute, second and day of week) (* Notes 6 and 7)</td></tr>
<tr><td>Link functions</td><td colspan="3">Inter−PLC link, computer link, remote programming, modem and data transfer</td></tr>
<tr><td>Self-diagnostic functions</td><td colspan="3">Watchdog timer, memory malfunction detection, I/O malfunction detection, backup battery malfunction detection, program syntax check, etc.</td></tr>
<tr><td>Other functions</td><td colspan="3">ROM operation function (* Note 8), program block edition during RUN mode, forced input/output, interrupt processing, test run, constant scan and machine language program</td></tr>
<tr><td rowspan="5">Memory backup time (lithium battery storage time)</td><td colspan="2">CPU only</td><td>Min. 10,000 hours
(typical: approx. 13,000 hours)</td></tr>
<tr><td rowspan="4">When installed expansion memory unit</td><td>FP2−EM1</td><td>Min. 9,000 hours
(typical: approx. 12,000 hours)</td></tr>
<tr><td>FP2−EM2,
FP2−EM3</td><td>Min. 8,000 hours
(typical: approx. 12,000 hours)</td></tr>
<tr><td>FP2−EM6</td><td>Min. 8,500 hours
(typical: approx. 12,500 hours)</td></tr>
<tr><td>FP2−EM7</td><td>Min. 10,000 hours
(typical: approx. 13,000 hours)</td></tr>
</table>

☞ Notes

1) **The practical usable external input and output points are restricted according to the number of the input and output units. The external output relays (Y) that not used at the output unit can be used as internal relays.**
2) **The expansion memory unit (FP2−EM2, FP2−EM3 or FP2−EM6) is required.**
3) **Hold or non-hold type can be set using the system registers.**
4) **Can also be used as internal relays.**
5) **Can also be used as data registers.**
6) **The expansion memory unit (FP2−EM1, FP2−EM2 or FP2−EM3) is required.**
7) **Precision of calendar timer:**
   At 0°C/32°F, less than 90-second error per month.
   At 25°C/77°F, less than 40-second error per month.
   At 55°C/131°F, less than 98-second error per month.
8) **The expansion memory unit (FP2−EM3, FP2−EM6 or FP2−EM7) is required.**

FP2SH Performance Specifications

Item		FP2SH CPU FP2–C2L (AFP2221), FP2–C2 (AFP2231), FP2–C2P (AFP2235), FP2–C3P (AFP2255)
Program/control method		Relay symbol/cyclic operation
Controllable I/O points	**Basic construction**	Using Backplanes: Max. 768 points (12 modules) Using Backplanes H type: Max. 512 points (8 modules)
	Expanded construction	Using Backplanes: Max. 1,600 points (25 modules) Using Backplanes H type: Max. 2,048 points (32 modules)
	Using remote I/O system	Max. 8,192 points (using S–LINK or MEWNET-F system)
Program capacity	**Internal memory**	FP2–C2/FP2–C2P: approx. 60K steps FP2–C3P: approx. 120K steps
	Using expansion memory unit	——
Number of instructions	**Basic instructions**	95 types
	High-level instructions	434 types
Operation speed (typical value)	**Basic instructions**	From 0.03μs per instruction
	High-level instructions	From 0.06μs per instruction
Operation memory points for relays	**External input relays (X)**	8,192 points (* Note 1)
	External output relays (Y)	8,192 points (* Note 1)
	Internal relays (R)	14,192 points (* Note 2)
	Timer/counter (T/C)	Total 3,072 points (* Note 2) – Timer: units of 1ms, 10ms, 100ms and 1s counts up to 32,767 × each unit – Counter: 1 to 32,767 counts
	Link relays (L)	10,240 points (* Notes 2 and 3)
	Pulse relays (P)	2,048 points (* Note 2)
	Alarm relays (E)	2,048 points (* Note 2)
Operation memory points for memory areas	**Data registers (DT)**	10,240 words (* Note 2)
	File registers (FL)	FP2–C2L: 32,765 words FP2–C2, FP2–C2P, FP2–C3P: 32,765 words × 3 banks (* Note 2)
	Link data registers (LD)	8,448 words (* Notes 2 and 4)
	Timer/counter set value area (SV)	3,072 words
	Timer/counter elapsed value area (EV)	3,072 words
	Index registers (I0 to ID)	14 words × 16 banks

Item	FP2SH CPU	
	FP2−C2L (AFP2221), FP2−C2 (AFP2231), FP2−C2P (AFP2235), FP2−C3P (AFP2255)	
Differential points	Unlimited number of points	
Auxiliary timer	Unlimited number of points, down type timer (0.01 to 327.67s)	
Shift register	Max. 887 points	
Master control relay points (MCR)	256 points (For FP2−C3P: 1st program: 256 points/2nd program: 256 points)	
Number of labels (JP and LOOP)	256 points (For FP2−C3P: 1st program: 256 points/2nd program: 256 points)	
Number of step ladder	1,000 steps (For FP2−C3P: 1st program only)	
Number of subroutine	100 subroutines	
Number of interrupt program	25 program	
Comment input function	Available (internal function)	
Clock/calendar function	Available (year, month, day, hour, minute, second and day of week) (* Note 5)	
Link functions	Inter−PLC link, computer link, remote programming, modem and data transfer	
Self-diagnostic functions	Watchdog timer, memory malfunction detection, I/O malfunction detection, back-up battery malfunction detection, program syntax check, etc.	
Other functions	ROM operation function (* Note 6) forced input/output, interrupt processing, test run and constant scan	
Memory backup time (lithium battery storage time)	CPU only	Min. 3,500 hours or more (typical: approx. 31,000 hours)
	When installing memory unit (AFP2207 or AFP2208)	Min. 3,500 hours (typical: approx. 31,000 hours)
Memory backup time for IC memory card (at 25 °C)	AIC52000 (Rechargeable type)	3 months or more (After full charge)
	AFP2209 (Interchangeable type)	3 years or more

Notes

1) The practical usable external input and output points are restricted according to the number of the input and output units.
2) Hold or non-hold type can be set using the system registers.
3) Can also be used as internal relays.
4) Can also be used as data registers.
5) Precision of calendar timer:
   At 0°C/32°F, less than 57-second error per month.
   At 25°C/77°F, less than 88-second error per month.
   At 55°C/131°F, less than 88-second error per month.
6) For FP2−C2L and FP2−C2, the memory unit is required.

10.2 Relays, Memory Areas and Constants

Item		Function	Numbering	
			FP2	FP2SH
Relay	External input relay (X)	Turn on or off based on external input.	2,048 points (X0 to X127F)	8,192 points (X0 to X511F)
	External output relay (Y)	Externally outputs on or off state.	2,048 points (Y0 to Y127F)	8,192 points (Y0 to Y511F)
	Internal relay(R) (* Note 1) (R)	Relay which turns on or off only within program.	4,048 points (R0 to R252F)	14,192 points (R0 to R886F)
	Link relay (* Note 1) (L)	This relay is a shared relay used for MEWNET link system.	2,048 points (L0 to L127F)	10,240 points (L0 to L639F)
	Timer (* Notes 1 and 2) (T)	If a **TM** instruction has timed out, the contact with the same number turns on.	1,024 points (T0 to T999/ C1000 to C1023)	3,072 points (T0 to T2999/ C3000 to C3071)
	Counter (* Notes 1 and 2) (C)	If a **CT** instruction has counted up, the contact with the same number turn on.		
	Pulse relay (P)	This relay is used to turn on only for one scan duration programmed with the **OT**" and **OT**# instructions.	1,024 points (P0 to P63F)	2,048 points (P0 to P127F)
	Error alarm relay (E)	If turned on while the unit is running, this relay stores the history in a dedicated buffer. Program this relay so that it is turned on at the time of abnormality.	—	2,048 points (E0 to E2047)
	Special internal relay (R)	Relay which turns on or off based on specific conditions and is used as a flag.	176 points (R9000 to R910F)	176 points (R9000 to R910F)

Item		Function	Numbering	
			FP2	FP2SH
Memory area	**External input relay (WX)**	Code for specifying 16 external input points as one word (16 bits) of data.	128 words (WX0 to WX127)	512 words (WX0 to WX511)
	External output relay (WY)	Code for specifying 16 external output points as one word (16 bits) of data.	128 words (WY0 to WY127)	512 words (WY0 to WY511)
	Internal relay (WR)	Code for specifying 16 internal relay points as one word (16 bits) of data.	253 words (WR0 to WR252)	887 words (WR0 to WR886)
	Link relay (WL)	Code for specifying 16 link relay points as one word (16 bits) of data.	128 words (WL0 to WL127)	640 words (WL0 to WL639)
	Data register (* Note 1) (DT)	Data memory used in program. Data is handled in 16-bit units (one word).	6,000 words (DT0 to DT5999)	10,240 words (DT0 to DT10239)
	Link data register (* Note 1) (LD)	This is a shared data memory which is used within the MEWNET link system. Data is handled in 16-bit units (one word).	256 words (LD0 to LD255)	8,448 words (LD0 to LD8447)
	Timer/Counter set value area (* Note 1) (SV)	Data memory for storing a target value of a timer and an initial value of a counter. Stores by timer/counter number.	1,024 words (SV0 to SV1023)	3,072 words (SV0 to SV3071)
	Timer/Counter elapsed value area (Note 1 and Note 3) (EV)	Data memory for storing the elapsed value during operation of a timer/counter. Stores by timer/ counter number.	1,024 words (EV0 to EV1023)	3,072 words (EV0 to EV3071)
	File register (* Notes 1 and 3) (FL)	Data memory used in program. Data is handled in 16-bit units (one word).	FP2 (16 K): 0 to 14,333 words (FL0 to FL14332) FP2 (32 K) (when expanded): 0 to 30,717 words (FL0 to FL30716)	FP2−C2L: 32,765 words FP2−C2, FP2−C2P, FP2−C3P: 32,765 words × 3 banks
	Special data register (DT)	Data memory for storing specific data. Various settings and error codes are stored.	256 words (DT90000 to DT90255)	512 words (DT90000 to DT90511)
	Index register (I)	Register can be used as an address of memory area and constants modifier.	14 words (I0 to ID)	14 words × 16 banks (I0 to ID)

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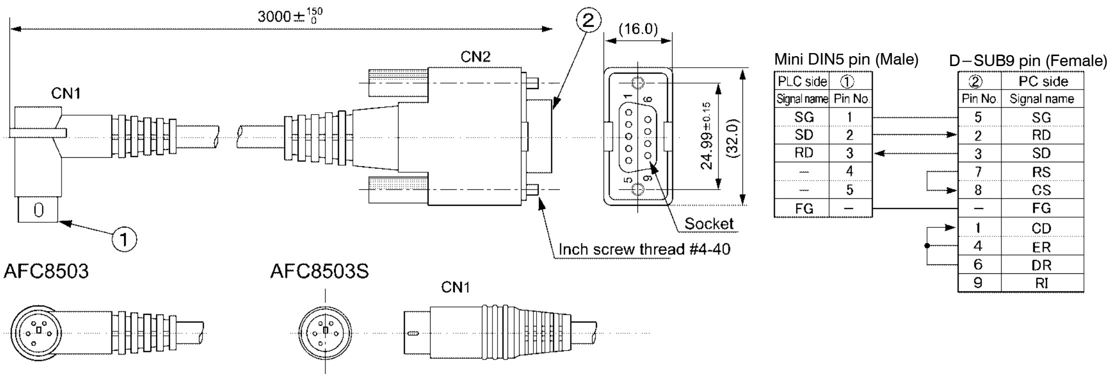
Item		Numbering
		FP2/FP2SH
Control instruction point	Master control relay points (MCR)	256 points
	Number of labels (JP and LOOP)	Total: 256 points
	Number of step ladder (* Note 4)	1,000 steps
	Number of subroutine	100 subroutines
	Number of interrupt program	1 program (periodical interrupt: allows setting of the time interval within the range from 0.5ms to 1.5s)
Constant	Decimal constants (K)	K−32768 to K32767 (for 16-bit operation)
		K−2147483648 to K2147483647 (for 32-bit operation)
	Hexadecimal constants (H)	H0 to HFFFF (for 16-bit operation)
		H0 to HFFFFFFFF (for 32-bit operation)
	Decimal constants (monorefined real number) (f)	f−1.175494 $\times$ 10^{-38} to f−3.402823 $\times$ 10^{38} f1.175494 $\times$ 10^{-38} to f3.402823 $\times$ 10^{38}

Notes

1) **There are two unit types, the hold type that saves the conditions that exist just before turning the power off or changing from the RUN mode to PROG. mode, and the non-hold type that resets them. The selection of hold type and non-hold type can be changed by the setting of system register.**
2) **The points for the timer and counter can be changed by the setting of system register 5. The numbers given in the table are numbers when system register 5 is at its default setting.**
3) **The size of the file register varies depending on the settings of system registers 0, 1 and 2.**
4) **Hold or non-hold type can be set using the system registers.**

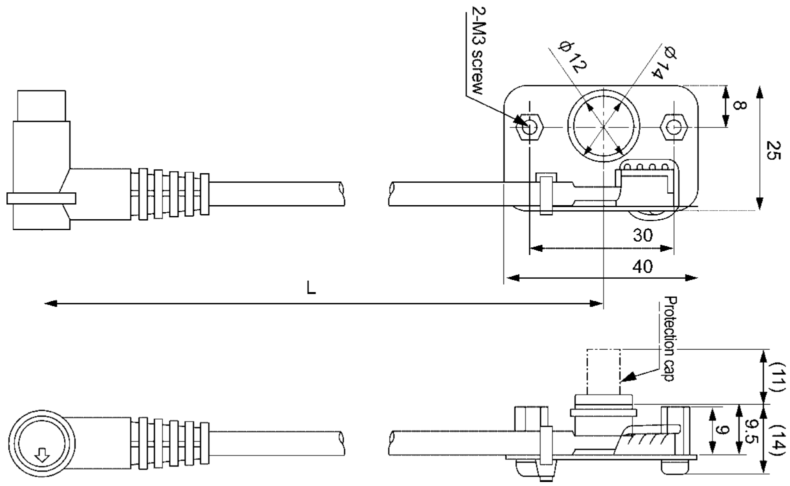
10.3 Cable/Adapter Specifications

10.3.1 AFC8503/AFC8503S



(Unit: mm)

10.3.2 AFC85305/AFC8531/AFC8532 (For extending for the tool port)



	L (mm)
AFC85305	$500\pm^{100}_{0}$
AFC8531	$1000\pm^{100}_{0}$
AFC8532	$2000\pm^{100}_{0}$

(Unit: mm)
(Unit: mm)

10.3 Cable/Adapter Specifications

Chapter 11

Appendix

11.1 System Registers / Special Internal Relays / Special Data Registers

Precaution for System Registers

What is the system register area

- System registers are used to set values (parameters) which determine operation ranges and functions used. Set values based on the use and specifications of your program.
- There is no need to set system registers for functions which will not be used.

Type of system registers

The registers to be used depend on each PLC.

(1) Allocation of user memory (System registers 0, 1 and 2)

These registers set the size of the program area and file register area, allowing the user memory area to be configured for the environment used. The size of the memory area will vary depending on the type.

(2) Allocation of timers and counters (System register 5)

The number of timers and counters is set by specifying the starting counter number.

(3) Hold/non-hold type setting (System registers 6 to 18)

When these registers are set to “hold type”, the values in the relays and data memory will be retained even if the system is switched to PROG. mode or the power is turned off. If set to “non-hold type”, the values will be cleared to “0”.

(4) Operation mode setting on error (System registers 4, 20 to 28)

Set the operation mode when errors such as battery error, duplicated use of output, I/O verification error and operation error occur.

(5) Time settings (System registers 29 to 34)

Set time-out error detection time and the constant scan time.

(6) Remote I/O operation settings (System registers 25, 35 and 36)

These registers are used to select whether or not to wait for a slave station connection when the remote I/O is started, and the remote I/O update timing.

(7) MEWNET-W PLC link settings (System registers 40 to 47, 50 to 55, and 57)

These settings are for using link relays and link registers for MEWNET-W PC(PLC) link communication.
Note) The default value setting is “no PC(PLC) link communication”.

(8) Tool and COM port communication settings (System registers 410 to 418)

Set these registers when the Tool port and COM port are to be used for computer link, general-purpose serial communication, PC(PLC) link, and modem communication. Note that the default setting is computer link mode.

Checking and changing the set value of system register

If you are going to use a value which is already set (the value which appears when read), there is no need write it again.

Using programming tool software

Produce:

1. Set the control unit in the PROG mode.
2. Option ->PLC Configuration
3. When the function for which setting are to be entered is selected in the PLC Configuration dialog box, the value and setting status for the selected system register are displayed.
   To change the value and setting status, write in the new value and /or select the setting status.
4. To register these settings, choose OK

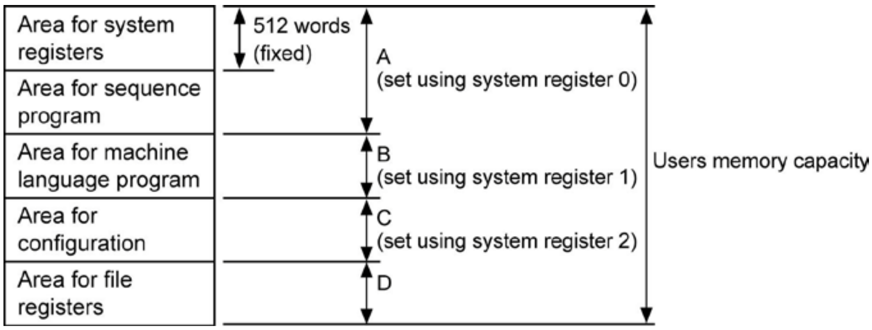
Precautions for system register setting

- System register settings are effective from the time they are set. However, input settings, tool portico port, and modem connection settings become effective when the mode is changed from PROG. to RUN.
- With regard to the modem connection setting, when the power is turned off and on or when the mode is changed from PROG. to RUN, the controller sends a command to the modem which enables it for reception.
- When the initialized operation is performed, all set system register values (parameters) will be initialized

11.1.1 Table of System Registers for FP2/FP2SH/FP10SH

Allocation of user memory (system registers 0, 1 and 2)
Available PLC: FP2

The configuration of user memory of FP2 is as follows:



Be sure to set the A (using system register 0), B (using system register 1), and C (using system register 2) as even numbers.
The area remaining in A after 512 words are subtracted is the sequence program area that can actually be used.
File register area D is the area that remains after A, B, and C have been subtracted from the user memory capacity.
The configuration area is reserved for future expansion.

FP2 (16K)

Users memory capacity : 16K words
Setting range of A : 2K to 16K words (default value: 12k)
Setting range of B : 0 to 14K words (default value: 0)
Setting range of C : 0 to 14K words (default value: 0)
Allocate so that A+B+C≧16

Setting example: The values of D when B = C = 0.

A	Area for sequence program (1024 x A-512)	Area for file registers (D)
2	1,535 steps	14,333 words
4	3,583 steps	12,285 words
6	5,631 steps	10,237 words
8	7,679 steps	8,189 words
10	9,727 steps	6,141 words
12	**11,775 steps (default value)**	**4,093 words (default value)**
14	13,823 steps	2,045 words
16	15,871 steps	0 word

FP2 (32K)

Users memory capacity	: 32K words
Setting range of A	: 2K to 32K words (default value: 12k)
Setting range of B	: 0 to 30K words (default value: 0)
Setting range of C	: 0 to 30K words (default value: 0)

Allocate so that A + B + C ≦ 32.

Setting example: The values of D when B = C = 0.

A	Area for sequence program (1024 x A-512)	Area for file registers (D)
2	1,535 steps	30,717 words
4	3,583 steps	28,669 words
6	5,631 steps	26,621 words
8	7,679 steps	24,573 words
10	9,727 steps	22,525 words
12	**11,775 steps (default value)**	**20,477 words (default value)**
14	13,823 steps	18,429 words
16	15,871 steps	16,381 words
18	17,919 steps	14,333 words
20	19,967 steps	12,285 words
22	22,015 steps	10,237 words
24	24,063 steps	8,189 words
26	26,111 steps	6,141 words
28	28,159 steps	4,093 words
30	30,207 steps	2,045 words
32	32,255 steps	0 word

Setting example for each area
When not using the machine language program area
Refer to the tables for the different types given above.

When using the machine language program area

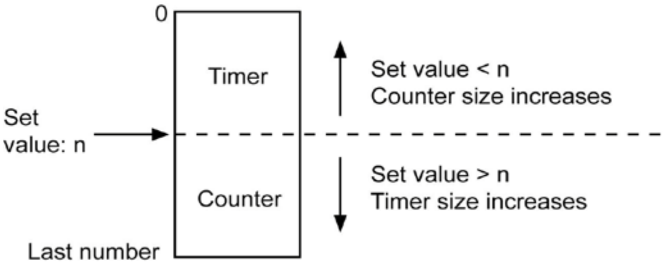
A	Area for machine language program
2	4,096 words
4	8,192 words
6	12,288 words
8	16,384 words
10	20,480 words
12	24,576 words
14	28,672 words
16	32,768 words

B	Area for machine language program
18	36,864 words
20	40,960 words
22	45,056 words
24	49,152 words
26	53,248 words
28	57,344 words
30	61,440 words

For example, for the FP2 (16K-step type), when the area for the sequence program (A) is set to 10K words and the area for configuration (C) is set to 0K words, the area for the machine language program can be set up to 6K words.

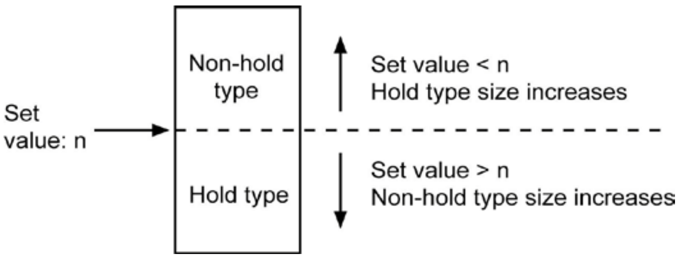
Setting the number of timers and counter (system register 5)
Timers and counters share the same area. If the method of dividing the area is changed, the number of timers and counters will also change.

Type	Total point numbers	Default value of system register 5	Timer	Counter
FP2	1,024 points	1000	1000 points (No. 0 to 999)	24 points (No. 1000 to 1023)
FP2SH/FP10SH	3,072 points	3000	3000 points (No. 0 to 2999)	72 points (No. 3000 to 3071)



- For FP2/FP2SH, set the system registers 5 and 6 to the same value. This sets the timer to a non-hold type and counter to a hold type.
- By setting system register 5 to “0”, the whole area becomes the counter. Also, by setting it to the value 1 higher than the last number, the whole area becomes the timer.

Hold type area starting address (system registers 6 to 13)
Set each relay and register to a hold type or non-hold type.



- For normal situations, set the system registers 5 and 6 to the same value. This sets the timer to a non-hold type and counter to a hold type.
- By setting this value to the first number, the whole area becomes hold type. Also, by setting it to the value 1 higher than the last number, the whole area becomes non-hold type.
- The relays and registers for links not specified in the send area of system registers 40 to 55 are non-hold type regardless of what is set here.

- For the FP2SH/FP10SH, the index registers can be set to hold type or non-hold type. The register numbers and settings are related as shown below.

Bank number	Set value for I0 to ID	Bank number	Set value for I0 to ID
Bank 0	0 to 13	**Bank 8**	112 to 125
Bank 1	14 to 27	**Bank 9**	126 to 139
Bank 2	28 to 41	**Bank A**	140 to 153
Bank 3	42 to 45	**Bank B**	154 to 167
Bank 4	56 to 69	**Bank C**	168 to 181
Bank 5	70 to 83	**Bank D**	182 to 195
Bank 6	84 to 97	**Bank E**	196 to 209
Bank 7	98 to 111	**Bank F**	210 to 223

efault value of hold type area setting

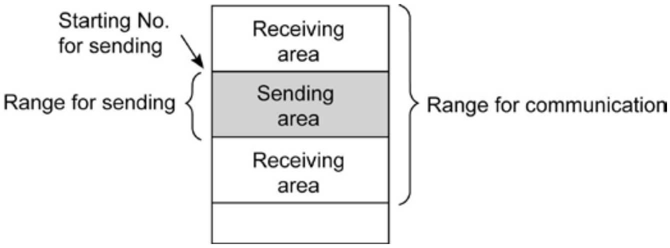
Type / Area	FP2	FP2SH
Timer	All non-hold type	
Counter	All hold type	
Internal relay	Non-hold type: 200 words (WR0 to WR199)	Non-hold type: 500 words (WR0 to WR499)
	Hold type: 53 words (WR200 to WR252)	Hold type: 387 words (WR500 to WR886)
Data register	All hold type	
File register	All hold type	
Link relay for MEWNET-W	All hold type	
Link register for MEWNET-W	All hold type	
Index register	-	All hold type

Type / Area	FP10SH
Timer	All non-hold type
Counter	All hold type
Internal relay	Non-hold type: 500 words (WR0 to WR499)
	Hold type: 387 words (WR500 to WR886)
Data register	All hold type
File register	All hold type
Link relay for MEWNET-W/P	All hold type
Link register for MEWNET-W/P	All hold type
Link relay for MEWNET-H	All hold type
Link register for MEWNET-H	All hold type
Index register for FP10SH	All hold type

MEWNET-W PC link setting

For PC link (W) 0: System registers 40 to 45
For PC link (W) 1: System registers 50 to 55

Regarding the link relays and link data registers, specify the range for communication and divide it up for sending and receiving.



- The default settings have the range for communication (system registers 40, 41, 50 and 51) set to 0 so that PC link communication is not possible.
- If the range for sending (system registers 43, 45, 53 and 55) is set to 0, the range for communication will all be for receiving.
- The link relay and link data register ranges not used for communication, can each be used as internal relays and data registers.

Table of system registers for FP2/FP2SH/FP10SH

<table>
<tr><th>Item</th><th>Add-
ress</th><th colspan="2">Name</th><th>Default value</th><th>Descriptions</th></tr>
<tr><td rowspan="3">Alloca-
tion of
user
memory</td><td>0</td><td colspan="2">Sequence program area capacity setting
Available PLC: FP2</td><td>12K words</td><td>FP2 (16K): 2 to 16K words
FP2 (32K): 2 to 32K words</td></tr>
<tr><td>1</td><td colspan="2">Machine language program area capacity setting
Available PLC: FP2</td><td>0 word</td><td>FP2 (16K): 0 to 14K words
FP2 (32K): 0 to 30K words</td></tr>
<tr><td>2</td><td colspan="2">Configuration capacity setting
Available PLC: FP2</td><td>0 word</td><td>FP2 (16K): 0 to 14K words
FP2 (32K): 0 to 30K words</td></tr>
<tr><td rowspan="12">Action
on error</td><td rowspan="12">4</td><td colspan="2">Battery error alarm</td><td>Enabled</td><td>Enabled: When a battery error occurs, a self-diagnostic error is issued and the ERROR LED lights. (BATT. LED lights.)
Disabled: When a battery error occurs, a self-diagnostic error is not issued and the ERROR LED does not light. (BATT. LED does not light.)</td></tr>
<tr><td rowspan="8">Memory area contents setting at INITIALIZE position</td><td>Internal relay (R)</td><td>Cleared</td><td rowspan="8">Cleared: When the initialize/ test switch is set to INITIALIZE position while in the PROG. mode, you can specify the type of memory to be cleared.
Not cleared: When the initialize/test switch is set to INITIALIZE position while in the PROG. mode, you can specify the type of memory to be not cleared</td></tr>
<tr><td>Link relay (L)</td><td>Cleared</td></tr>
<tr><td>Timers/ Counters (T, C, SV, EV)</td><td>Cleared</td></tr>
<tr><td>Data register (DT)</td><td>Cleared</td></tr>
<tr><td>Link data register (LD)</td><td>Cleared</td></tr>
<tr><td>File register (FL)</td><td>Cleared</td></tr>
<tr><td>Index register (I)</td><td>Cleared</td></tr>
<tr><td>Error alarm relay (E)</td><td>Cleared</td></tr>
<tr><td colspan="2">Differential type instructions setting between MC and MCE instructions</td><td>Conven-
tional</td><td>Conventional: Holds preceded result in the MC and MCE instruction set.
New: Disregards preceded result in the MC and MCE instruction set.</td></tr>
<tr><td colspan="2">TM instruction operation setting
Available PLC: FP2SH, FP10SH</td><td>Conven-
tional</td><td>Conventional: Scan synchronous
New: Scan asynchronous</td></tr>
<tr><td colspan="2">Index modifier check setting</td><td>Enabled</td><td>Enabled: Checks for overflow of the index modifier area, and performs normal processing.
Disabled: Performs processing without checking for overflow of the index modifier area.</td></tr>
</table>

Note) The error alarm relay is available for FP2SH and FP10SH.

FP2/FP2SH/FP10SH

Item	Add-ress	Name	Default value	Descriptions
Hold/ Non-hold	**5**	**Counter starting address (setting the number of timers and counters)**	FP2SH/ FP10SH: 3000 FP2: 1000	FP2SH/ FP10SH: 0 to 3072 FP2: 0 to 1024 Set the system registers 5 and 6 to the same value.
	6	**Hold type area starting address setting for timer/counter**	FP2SH/ FP10SH: 3000 FP2: 1000	FP2SH/ FP10SH: 0 to 3072 FP2: 0 to 1024 Set the system registers 5 and 6 to the same value.
	7	**Hold type area starting address setting for internal relays (in word units)**	FP2SH/ FP10SH: 500 FP2: 200	FP2SH/FP10SH: 0 to 887 FP2: 0 to 253
	8	**Hold type area starting address setting for data registers**	0	FP2SH/FP10SH: 0 to 10240 FP2: 0 to 6000
	9	**Hold type area starting address setting for file registers (For FP2SH, bank 0)**	0	FP2SH/FP10SH: 0 to 32765 FP2 (16K): 0 to 14333 FP2 (32K): 0 to 30717
	10	**Hold type area starting address setting for MEWNET-W/P link relays (for PC link 0) (*Note)**	0	0 to 64
	11	**Hold type area starting address setting for MEWNET-W/P link relays (for PC link 1) (*Note)**	64	64 to 128
	12	**Hold type area starting address setting for MEWNET-W/P link data registers (for PC link 0) (*Note)**	0	0 to 128
	13	**Hold type area starting address setting for MEWNET-W/P link data registers (for PC link 1) (*Note)**	128	128 to 256
	14	**Hold or non-hold setting for step ladder process**	Non-hold	Hold/non-hold
	15	**Hold type area starting address setting for file register (for bank 1)**	0	0 to 32765

Note) Available PLC MEWNET-W: FP10SH, FP2, FP2SH
MEWNET-P: FP10SH

FP2/FP2SH/FP10SH

Item	Add-ress	Name	Default value	Descriptions
Hold/ Non-hold	16	**Hold type area starting address setting for MEWNET-H link relays Available PLC: FP10SH**	128	128 to 640
	17	**Hold type area starting address setting for MEWNET-H link data registers Available PLC: FP10SH**	256	256 to 8448
	18	**Hold type area starting address setting for index register Available PLC: FP2SH/ FP10SH**	0	0 to 224
	19	**Hold type area starting address setting for file register (for bank 2) Available PLC: FP2SH**	0	0 to 32765
Action on error	20	**Disable or enable setting for duplicated output**	Disable	Disable/enable
	21	**Operation settings when MEWNET-TR communication error occurs**	Stop	Stop/continuation
		Operation setting when I/O error occurs	Stop	Stop/continuation
	22	**Operation settings when an intelligent unit error occurs**	Stop	Stop/continuation
	23	**Operation settings when an I/O verification error occurs**	Stop	Stop/continuation
	24	**Operation settings when a system watching dog timer error occurs Available PLC: FP2SH/ FP10SH**	Stop	Stop/continuation Set the time-out time for watching dog timer with system register 30.
	25	**Operation settings when connection time error occurs in the remote slave station**	Stop	Stop/continuation
	26	**Operation settings when an operation error occurs**	Stop	Stop/continuation
	27	**Operation settings when communication error occurs in the MEWNET-F system**	Stop	Stop/continuation
	28	**Operation settings when error occurs in the slave station of the MEWNET-F system**	Stop	Stop/continuation

FP2/FP2SH/FP10SH

Item	Add-ress	Name	Default value	Descriptions
Time setting for FP2SH/ FP10SH	**29**	**Operation time setting for communication processing**	240 μs	0 to 52428 μs If the response of the connected programmable display is show, please make the value bigger.
	30	**Time-out time setting of system watching dog timer**	100 ms	0.4 to 640 ms
	31	**Multi-frame communication time settings in the computer link and communication time setting for data sending buffer**	6500 ms	10 to 81917.5 ms
	32	**Time-out time setting for the F145 (SEND)/P145 (PSEND), F146 (RECV)/P146 (PRECV), F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/P153 (PRMWT) instructions**	10000 ms	10 to 81917.5 ms
	33	**Effective time setting for monitoring**	163837.5 ms	2500 to 163837.5 ms
	34	**Constant scan time setting**	0 ms: Normal scan	0 to 640 ms: Scans once each specified time interval. Set “0”: Normal scan Setting time can be obtained using the formula “Set time” = “Set value” x 0.1 (ms)
Time setting for FP2	**31**	**Multi-frame communication time settings in the computer link**	6500 ms	10.0 to 8190.0 ms
	32	**Time-out time setting for the F145 (SEND)/P145 (PSEND), F146 (RECV)/P146 (PRECV), F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/P153 (PRMWT) instructions**	2000 ms	10.0 to 8190.0 ms
	33	**Program block-editing time in the RUN mode**	10000 μs	800.0 to 52428.0 μs
	34	**Constant scan time setting**	0 : Normal scan	0 to 640 ms: Scans once each specified time interval. Set “0”: Normal scan

FP2/FP2SH/FP10SH

Item	Add-ress	Name		Default value	Descriptions
Remote I/O control	**25**	**Operation settings when connection time error occurs in the remote slave station Available PLC: FP2SH**		Stop	Stop/continuation
	35	**Operation mode setting when the MEWNET-F system is used**		Enabled (wait for connec-tion)	Enabled: CPU starts operation after all the salve stations are recognized. Disabled: CPU starts operation without waiting for slave station connections. Only effective when registering remote I/O allocation.
	36	**I/O data updating mode settings for MEWNET-F system**		Scan syn-chronous	Scan asynchronous mode/ Scan synchronous mode
PC link 0 setting	**40**	**PC link 0 settings for MEWNET-W/-P link system (*Note)**	**Size of link relays used for commu-nication**	0	0 to 64 words
	41		**Size of link data registers used for commu-nication**	0	0 to 128 words
	42		**Send area starting address of link relay**	0	0 to 63
	43		**Size of link relays used for send area**	0	0 to 64 words
	44		**Send area starting address of link data register**	0	0 to 127
	45		**Size of link data registers used for send area**	0	0 to 127 words
	46	**PC link 0 and 1 allocation setting for MEWNET-W/-P link system (*Note)**		Normal allocation	Normal allocation: (PC link 0 for the link unit with a smaller slot number and PC link 1 for one with a larger slot number) Reverse allocation: (PC link 1 for the link unit with a smaller slot number and PC link 0 for one with a larger slot number)

Note) Available PLC MEWNET-W: FP10SH, FP2, FP2SH
MEWNET-P: FP10SH

FP2/FP2SH/FP10SH

Item	Add-ress	Name		Default value	Descriptions
MEWNET -H setting	**49**	**Processing capacity setting for PC link of MEWNET-H link system Available PLC: FP10SH**		4 (1024 bytes per scan)	0: All data in a scan 1 to 65535: Setting processing capacity per scan can be obtained using the formula "Capacity" = "Set value" x 256 bytes
PC link 1 setting	**50**	**PC link 1 settings for MEWNET-W/-P link system (*Note)**	**Size of link relays used for commu-nication**	0	0 to 64 words
	51		**Size of link data registers used for commu-nication**	0	0 to 128 words
	52		**Send area starting address of link relay**	64	64 to 127
	53		**Size of link relays used for send area**	0	0 to 64 words
	54		**Send area starting address of link data register**	128	128 to 255
	55		**Size of link data registers used for send area**	0	0 to 127 words
Tool port setting	**410**	**Unit number setting for tool port Available PLC: FP2/ FP2SH**		1	1 to 99 (unit No. 1 to 99)
	411	**Communication format setting for tool port Available PLC: FP2/ FP2SH**		Commu-nication format (character bit): 8 bits, Modem communi-cation: Disabled	Character bits: 7 bits/8bits Modem communication: Enabled/Disabled When connecting a modem, set the unit number to 1 with system register 410.

Note) Available PLC MEWNET-W: FP10SH, FP2, FP2SH
MEWNET-P: FP10SH

FP2/FP2SH/FP10SH

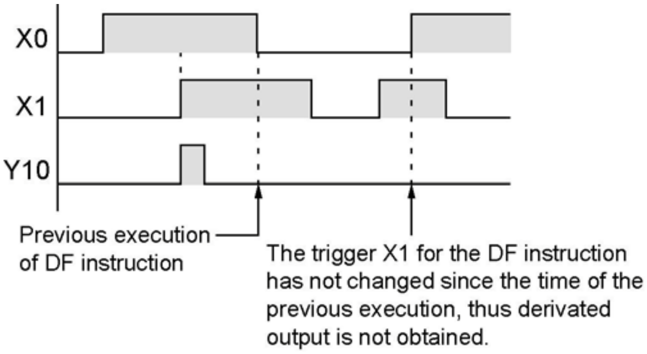
<table>
<tr><th>Item</th><th>Add-
ress</th><th>Name</th><th>Default value</th><th colspan="2">Descriptions</th></tr>
<tr><td>Tool port setting</td><td>414</td><td>Baud rate setting for the tool port</td><td>19200 bps</td><td colspan="2">In the FP10SH, when the dip switch SW1 on the CPU is off, the baud rate setting is effective.
In the FP2/FP2SH, when the dip switch SW1 on the rear of the CPU is off, the baud rate setting is effective.
19200 bps 19200 bps
1200 bps 38400 bps
2400 bps 57600 bps
4800 bps 115200 bps
9600 bps</td></tr>
<tr><td rowspan="5">COM port setting</td><td>412</td><td>Communication method setting for COM port</td><td>FP2: Not used
FP2SH/ FP10SH: Computer link</td><td colspan="2">UNUSED: COM port is not used.
COMPUTER LINK: computer link mode (when connecting C-NET)
GENERAL: serial data communication mode</td></tr>
<tr><td>413</td><td>Communication format setting (Common setting for both computer link and serial data communication)
When used for computer link, the start and end code settings of format for MEWTOCOL-COM will not be effective.
Available PLC: FP2/ FP2SH</td><td>Character bit: 8 bits,
Parity chk: “With, odd”
Stop bit: 1 bit,
End code: CR,
Start code: NO STX</td><td colspan="2">Character bit: 7 bits/8 bits
Parity chk: non/with odd/with even
Stop bit: 1 bit/2 bits
End code: CR/CR+LF/NON/ETX
Start code: NO STX/STX</td></tr>
<tr><td>414</td><td>Baud rate setting for the COM port
Available PLC: FP2/ FP2SH</td><td>19200 bps</td><td colspan="2">19200 bps 19200 bps
1200 bps 38400 bps
2400 bps 57600 bps
4800 bps 115200 bps
9600 bps</td></tr>
<tr><td>415</td><td>Unit number setting for COM port
Available PLC: FP2/ FP2SH</td><td>1</td><td colspan="2">1 to 99 (unit No. 1 to 99)</td></tr>
<tr><td>416</td><td>Modem compatibility setting for COM port
Available PLC: FP2/ FP2SH</td><td>Modem disabled</td><td colspan="2">Modem enabled/Modem disabled
When connecting a modem, set the unit number to 1 with system register 415.</td></tr>
<tr><td rowspan="2">General commu-nication setting</td><td>417</td><td>Starting address setting for received buffer of serial data communication mode (data register number)</td><td>0</td><td>FP2SH/FP10SH: 0 to 10240
FP2: 0 to 5999</td><td rowspan="2">For details about its usage, refer to the F144 (TRNS)/ P144 (PTRNS) instructions.</td></tr>
<tr><td>418</td><td>Capacity setting for received buffer of serial data communication mode (word number)</td><td>1024</td><td>0 to 1024</td></tr>
</table>

Operation of DF instruction between MC and MCE instructions

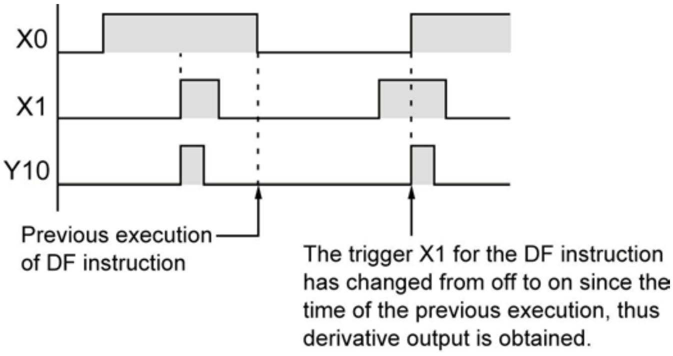
When a leading edge detection instruction (DF instruction) is used with the MC and MCE instructions, the derivative output may change as follows depending on the trigger of MC instruction and input timing of DF instruction. Take care regarding this point.

Example 1:
When system register 4 sets 0 (conventional)

Time chart 1

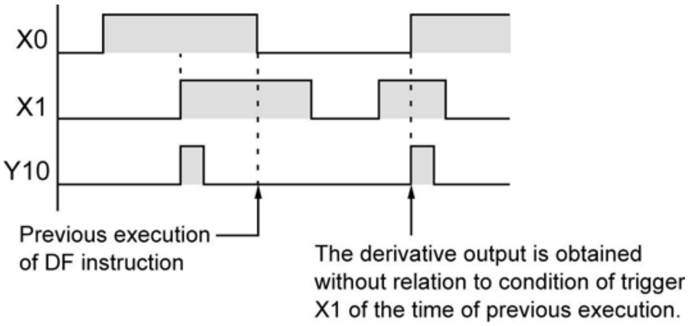


Time chart 2

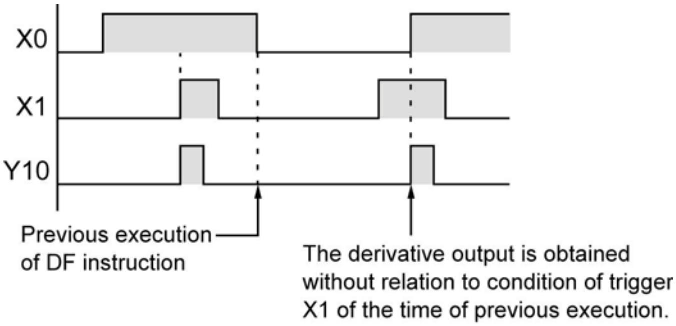


Example 2:
When system register 4 sets 1 (new)

Time chart 1



Time chart 2

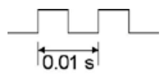
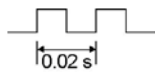
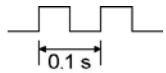
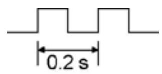
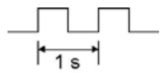
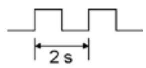
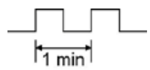


11.1.2 Table of Special Internal Relays for FP2/FP2SH/FP10SH

FP2/FP2SH/FP10SH

Address	Name	Description
R9000	**Self-diagnostic error flag**	Turns on when a self-diagnostic error occurs. The self-diagnostic error code is stored in DT90000.
R9001	**Not used**	-
R9002	**MEWNET-TR master error flag (Available PLC: FP10SH)**	Turns on when a communication error occurs in the MEWNET-TR master unit or MEWNET-TR network. The slot, where the erroneous MEWNET-TR master unit is installed, can be checked using DT90002 or DT90003.
	I/O error flag (Available PLC: FP2/ FP2SH)	Turns on when the error occurs in the I/O unit. The slot number of the unit where the error was occurred is stored in DT90002, DT90003.
R9003	**Intelligent unit error flag**	Turns on when an error occurs in an intelligent unit. The slot number, where the erroneous intelligent unit is installed is stored in DT90006 or DT90007.
R9004	**I/O verification error flag**	Turns on when an I/O verification error occurs. The slot number of the I/O unit where the verification error was occurred is stored in DT90010 or DT90011.
R9005	**Backup battery error flag (non-hold)**	Turns on for an instant when a backup battery error occurs.
R9006	**Backup battery error flag (hold)**	Turns on and keeps the on state when a backup battery error occurs. To reset R9006, - turn the power to off and then turn it on, - initialize, after removing the cause of error.
R9007	**Operation error flag (hold)**	Turns on and keeps the on state when an operation error occurs. The address where the error occurred is stored in DT90017. (Indicates the first operation error which occurred). FP2SH／FP10SH: When program is 120k steps and the higher byte of DT90257 is H2, the error occurs in the 2nd program block. In case of the 1st program block, it is H1.
R9008	**Operation error flag (non-hold)**	Turns on for an instant when an operation error occurs. The address where the operation error occurred is stored in DT90018 The contents change each time a new error occurs. FP2SH／FP10SH: When program is 120k steps and the higher byte of DT90258 is H2, the error occurs in the 2nd program block. In case of the 1st program block, it is H1.
R9009	**Carry flag**	Turns on for an instant, - when an overflow or underflow occurs. - when “1” is set by one of the shift instructions.
R900A	**> Flag**	Turns on for an instant when the compared results become larger in the “F60 (CMP)/P60 (PCMP), F61(DCMP)P61(PDCMP),F62 (WIN)/P62 (PWIN) or F63 (DWIN)/P63 (PDWIN) comparison instructions.”
R900B	**= Flag**	Turns on for an instant, - when the compared results are equal in the comparison instructions. - when the calculated results become 0 in the arithmetic instructions.

FP2/FP2SH/FP10SH

Address	Name	Description
R900C	**< Flag**	Turns on for an instant when the compared results become smaller in the “F60 (CMP)/P60 (PCMP), F61(DCMP)P61(PDCMP), F62 (WIN)/P62 ,(PWIN) or F63 (DWIN)/P63 (PDWIN) comparison instructions.”
R900D	**Auxiliary timer contact**	Turns on when the set time elapses (set value reaches 0) in the timing operation of the F137(STMR)/F183(DSTM) auxiliary timer instruction. The R900D turns off when the trigger for auxiliary timer instruction turns off.
R900E (*Note)	**Tool port error flag Available PLC: FP2SH**	Turns on when communication error at tool port is occurred.
R900F	**Constant scan error flag**	Turns on when the scan time exceeds the time specified in system register 34 during constant scan execution.
R9010	**Always on relay**	Always on.
R9011	**Always off relay**	Always off.
R9012	**Scan pulse relay**	Turns on and off alternately at each scan.
R9013	**Initial on pulse relay**	Turns on only at the first scan in the operation. Turns off from the second scan and maintains the off state.
R9014	**Initial off pulse relay**	Turns off only at the first scan in the operation. Turns on from the second scan and maintains the on state.
R9015	**Step ladder initial on pulse relay**	Turns on for an instant only in the first scan of the process the moment step ladder process is opened.
R9016, R9017	**Not used**	-
R9018	**0.01 s clock pulse relay**	Repeats on/off operations in 0.01 s cycles. 
R9019	**0.02 s clock pulse relay**	Repeats on/off operations in 0.02 s cycles. 
R901A	**0.1 s clock pulse relay**	Repeats on/off operations in 0.1 s cycles. 
R901B	**0.2 s clock pulse relay**	Repeats on/off operations in 0.2 s cycles. 
R901C	**1 s clock pulse relay**	Repeats on/off operations in 1 s cycles. 
R901D	**2 s clock pulse relay**	Repeats on/off operations in 2 s cycles. 
R901E	**1 min clock pulse relay**	Repeats on/off operations in 1 min cycles. 
R901F	**Not used**	-

Note) Used by the system.

FP2/FP2SH/FP10SH

Address	Name	Description
R9020	**RUN mode flag**	Turns off while the mode selector is set to PROG. Turns on while the mode selector is set to RUN.
R9021 (*Note)	**Test RUN mode flag**	Turns on while the initialize/test switch of the CPU is set to TEST and mode selector is set to RUN. (test run operation start) Turns off during the normal RUN mode.
R9022 (*Note)	**Break flag**	Turns on while the BRK instruction is executing or the step run is executing.
R9023 (*Note)	**Break enable flag**	Turns on while the BRK instruction is enabled in the test RUN mode.
R9024 (*Note)	**Output update enable flag in the test RUN mode**	Turns on while the output update is enabled in the test RUN mode.
R9025 (*Note)	**Single instruction flag**	Turns on while the single instruction execution is selected in the test RUN mode.
R9026 (*Note)	**Message flag**	Turns on while the F149 (MSG)/P149 (PMSG) instruction is executed.
R9027 (*Note)	**Remote mode flag**	Turns on while the mode selector is set to REMOTE.
R9028 (*Note)	**Break clear flag**	Turns on when the break operation is cleared.
R9029 (*Note))	**Forcing flag**	Turns on during forced on/off operation for I/O relay and timer/counter contacts.
R902A (*Note)	**External interrupt enable flag (Available PLC: FP2SH/FP10SH)**	Turns on while the external interrupt trigger is enabled by the ICTL instruction.
	Interrupt flag (Available PLC: FP2)	Turns on while the periodical interrupt is executed by the ICTL instruction.
R902B (*Note)	**Interrupt error flag**	Turns on when an interrupt error occurs.
R902C (*Note)	**Sampling point flag**	Turns off during instructed sampling. Turns on while sampling is triggered by the periodical interrupt.
R902D (*Note)	**Sampling trace end flag**	Turns on when the sampling trace ends.
R902E (*Note)	**Sampling trigger flag**	Turns on when the sampling trace trigger of the F156 (STRG)/P156 (PSTGR) instruction is turned on.
R902F (*Note)	**Sampling enable flag**	Turns on when the starting point of sampling is specified.

Note) Used by the system.

FP2/FP2SH/FP10SH

Address	Name	Description
R9030	**F145 (SEND)/P145 (PSEND) and F146 (RECV)/P146 (PRECV) instruction executing flag**	Monitors if CPU is in the F145 (SEND)/P145 (PSEND) and F146 (RECV)/P146 (PRECV) instructions executable condition as follows: - off: None of the above mentioned instructions can be executed. - on: One of the above mentioned instructions can be executed.
R9031	**F145 (SEND)/P145 (PSEND) and F146 (RECV)/P146 (PRECV) instruction end flag**	Monitors if an abnormality has been detected during the execution of the F145 (SEND)/P145 (PSEND) and F146 (RECV)/P146 (PRECV) instructions as follows: - off: No abnormality detected. - on: An abnormality detected. (communication error) The error code is stored in DT90039.
R9032	**COM port mode flag**	Monitors the mode of the COM port as: - on: Serial data communication mode - off: Computer link mode
R9033	**F147 (PR) instruction flag**	Turns on while a F147 (PR) instruction is executed. Turns off when a F147 (PR) instruction is not executed.
R9034	**Editing in RUN mode flag**	Turns on while editing a program in the RUN mode.
R9035	**F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/P153 (PRMWT) instruction execution flag**	Monitors if FP3/FP10SH is in the F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/P153 (PRMWT) instructions executable condition as follows: - off: None of the above mentioned instructions can be executed. - on: One of the above mentioned instructions can be executed.

FP2/FP2SH/FP10SH

Address	Name	Description
R9036	**F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/P153 (PRMWT) instruction end flag**	Monitors if an abnormality has been detected during the execution of the F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/P153 (PRMWT) instructions as follows: - off: No abnormality detected. - on: An abnormality detected. (access error) The error code is stored in DT90036.
R9037	**COM port communica-tion error flag**	Turns on when the serial data communication error occurs using COM port. Turns off when data is being sent by the F144 (TRNS) instruction.
R9038	**COM port receive flag**	Turns on when the end code is received during the serial data communicating.
R9039	**COM port send flag**	Turns on while data is not sent during the serial data communicating. Turns off while data is being sent during the serial data communicating.
R903A	**Not used**	-
R903B	**Not used**	-
R903C	**Not used**	-
R903D	**Not used**	-
R903E	**Not used**	-
R903F	**Not used**	-
R9040	**Error alarm (0 to 2047) Available PLC: FP2SH/FP10SH**	Turns on while the error alarm relay (E0 to E2047) acts. Turns off when the all error alarm relay turns off.

FP2/FP2SH/FP10SH

Address	Name	Description
R9050	**MEWNET-W/-P link transmission error flag [W/P LINK 1]**	When using MEWNET-W link unit or MEWNET-P link unit: - turns on when transmission error occurs at link 1. - turns on when there is an error in the link area settings.
R9051	**MEWNET-W/-P link transmission error flag [W/P LINK 2]**	When using MEWNET-W link unit or MEWNET-P link unit: - turns on when transmission error occurs at link 2. - turns on when there is an error in the link area settings.
R9052	**MEWNET-W/-P link transmission error flag [W/P LINK 3]**	When using MEWNET-W link unit or MEWNET-P link unit: - turns on when transmission error occurs at link 3. - turns on when there is an error in the link area settings.
R9053	**MEWNET-W/-P link transmission error flag [W/P LINK 4]**	When using MEWNET-W link unit or MEWNET-P link unit: - turns on when transmission error occurs at link 4. - turns on when there is an error in the link area settings.
R9054	**MEWNET-W/-P link transmission error flag [W/P LINK 5]**	When using MEWNET-W link unit or MEWNET-P link unit: - turns on when transmission error occurs at link 5. - turns on when there is an error in the link area settings.
R9055	**Not used**	-
R9056	**Not used**	-
R9057	**Not used**	-
R9058	**Remote I/O transmission error flag (master 1)**	When using MEWNET -F (remote I/O) system: - turns on when transmission error occurs on master 1. - turns on when there is an error in the settings.
R9059	**Remote I/O transmission error flag (master 2)**	When using MEWNET -F (remote I/O) system: - turns on when transmission error occurs on master 2. - turns on when there is an error in the settings.
R905A	**Remote I/O transmission error flag (master 3)**	When using MEWNET -F (remote I/O) system: - turns on when transmission error occurs on master 3. - turns on when there is an error in the settings.
R905B	**Remote I/O transmission error flag (master 4)**	When using MEWNET -F (remote I/O) system: - turns on when transmission error occurs on master 4. - turns on when there is an error in the settings.
R905C to R905F	**Not used**	-

FP2/FP2SH/FP10SH

Address	Name		Description
R9060	**MEWNET-W/ -P PC link transmission assurance relay [for PC link 0 (W/P)] (*Note)**	**Unit No.1**	Turns on when Unit No. 1 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9061		**Unit No.2**	Turns on when Unit No. 2 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9062		**Unit No.3**	Turns on when Unit No. 3 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9063		**Unit No.4**	Turns on when Unit No. 4 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9064		**Unit No.5**	Turns on when Unit No. 5 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9065		**Unit No.6**	Turns on when Unit No. 6 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9066		**Unit No.7**	Turns on when Unit No. 7 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9067		**Unit No.8**	Turns on when Unit No. 8 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9068		**Unit No.9**	Turns on when Unit No. 9 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9069		**Unit No.10**	Turns on when Unit No. 10 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R906A		**Unit No.11**	Turns on when Unit No. 11 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R906B		**Unit No.12**	Turns on when Unit No. 12 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R906C		**Unit No.13**	Turns on when Unit No. 13 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R906D		**Unit No.14**	Turns on when Unit No. 14 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R906E		**Unit No.15**	Turns on when Unit No. 15 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R906F		**Unit No.16**	Turns on when Unit No. 16 is communicating properly I n the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.

Note) When the system registers 46=K0, PC link 0 for the link unit with a smaller slot No. and PC link 1 for one with a larger slot No.
When the system registers 46=K1, PC link 1 for the link unit with a smaller slot No. and PC link 0 for one with a larger slot No.

FP2/FP2SH/FP10SH

Address	Name		Description
R9070	**MEWNET-W/-P PC link operation mode relay [for PC link 0 (W/P)]**	**Unit No.1**	Turns on when unit No. 1 is in the RUN mode. Turns off when unit No. 1 is in the PROG. mode.
R9071		**Unit No.2**	Turns on when unit No. 2 is in the RUN mode. Turns off when unit No. 2 is in the PROG. mode.
R9072		**Unit No.3**	Turns on when unit No. 3 is in the RUN mode. Turns off when unit No. 3 is in the PROG. mode.
R9073		**Unit No.4**	Turns on when unit No. 4 is in the RUN mode. Turns off when unit No. 4 is in the PROG. mode.
R9074		**Unit No.5**	Turns on when unit No. 5 is in the RUN mode. Turns off when unit No. 5 is in the PROG. mode.
R9075		**Unit No.6**	Turns on when unit No. 6 is in the RUN mode. Turns off when unit No. 6 is in the PROG. mode.
R9076		**Unit No.7**	Turns on when unit No. 7 is in the RUN mode. Turns off when unit No. 7 is in the PROG. mode.
R9077		**Unit No.8**	Turns on when unit No. 8 is in the RUN mode. Turns off when unit No. 8 is in the PROG. mode.
R9078		**Unit No.9**	Turns on when unit No. 9 is in the RUN mode. Turns off when unit No. 9 is in the PROG. mode.
R9079		**Unit No.10**	Turns on when unit No. 10 is in the RUN mode. Turns off when unit No. 10 is in the PROG. mode.
R907A		**Unit No.11**	Turns on when unit No. 11 is in the RUN mode. Turns off when unit No. 11 is in the PROG. mode.
R907B		**Unit No.12**	Turns on when unit No. 12 is in the RUN mode. Turns off when unit No. 12 is in the PROG. mode.
R907C		**Unit No.13**	Turns on when unit No. 13 is in the RUN mode. Turns off when unit No. 13 is in the PROG. mode.
R907D		**Unit No.14**	Turns on when unit No. 14 is in the RUN mode. Turns off when unit No. 14 is in the PROG. mode.
R907E		**Unit No.15**	Turns on when unit No. 15 is in the RUN mode. Turns off when unit No. 15 is in the PROG. mode.
R907F		**Unit No.16**	Turns on when unit No. 16 is in the RUN mode. Turns off when unit No. 16 is in the PROG. mode.

Note) When the system registers 46=K0, PC link 0 for the link unit with a smaller slot No. and PC link 1 for one with a larger slot No.
When the system registers 46=K1, PC link 1 for the link unit with a smaller slot No. and PC link 0 for one with a larger slot No.

FP2/FP2SH/FP10SH

Address	Name		Description
R9080	**MEWNET-W/-P PC link transmission assurance relay [for PC link 1 (W/P)] (*Note)**	**Unit No.1**	Turns on when unit No. 1 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9081		**Unit No.2**	Turns on when unit No. 2 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9082		**Unit No.3**	Turns on when unit No. 3 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9083		**Unit No.4**	Turns on when unit No. 4 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9084		**Unit No.5**	Turns on when unit No. 5 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9085		**Unit No.6**	Turns on when unit No. 6 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9086		**Unit No.7**	Turns on when unit No. 7 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9087		**Unit No.8**	Turns on when unit No. 8 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9088		**Unit No.9**	Turns on when unit No. 9 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R9089		**Unit No.10**	Turns on when unit No. 10 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R908A		**Unit No.11**	Turns on when unit No. 11 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R908B		**Unit No.12**	Turns on when unit No. 12 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R908C		**Unit No.13**	Turns on when unit No. 13 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R908D		**Unit No.14**	Turns on when unit No. 14 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R908E		**Unit No.15**	Turns on when unit No. 15 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.
R908F		**Unit No.16**	Turns on when unit No. 16 is communicating properly in the PC link mode. Turns off when operation is stopped, when an error occurs, or when not in the PC link mode.

Note) When the system registers 46=K0, PC link 0 for the link unit with a smaller slot No. and PC link 1 for one with a larger slot No.
When the system registers 46=K1, PC link 1 for the link unit with a smaller slot No. and PC link 0 for one with a larger slot No.

FP2/FP2SH/FP10SH

Address	Name		Description
R9090	**MEWNET-W/-P PC link operation mode relay [for PC link 1 (W/P)] (*Note)**	**Unit No.1**	Turns on when unit No. 1 is in the RUN mode. Turns off when unit No. 1 is in the PROG. mode.
R9091		**Unit No.2**	Turns on when unit No. 2 is in the RUN mode. Turns off when unit No. 2 is in the PROG. mode.
R9092		**Unit No.3**	Turns on when unit No. 3 is in the RUN mode. Turns off when unit No. 3 is in the PROG. mode.
R9093		**Unit No.4**	Turns on when unit No. 4 is in the RUN mode. Turns off when unit No. 4 is in the PROG. mode.
R9094		**Unit No.5**	Turns on when unit No. 5 is in the RUN mode. Turns off when unit No. 5 is in the PROG. mode.
R9095		**Unit No.6**	Turns on when unit No. 6 is in the RUN mode. Turns off when unit No. 6 is in the PROG. mode.
R9096		**Unit No.7**	Turns on when unit No. 7 is in the RUN mode. Turns off when unit No. 7 is in the PROG. mode.
R9097		**Unit No.8**	Turns on when unit No. 8 is in the RUN mode. Turns off when unit No. 8 is in the PROG. mode.
R9098		**Unit No.9**	Turns on when unit No. 9 is in the RUN mode. Turns off when unit No. 9 is in the PROG. mode.
R9099		**Unit No.10**	Turns on when unit No. 10 is in the RUN mode. Turns off when unit No. 10 is in the PROG. mode.
R909A		**Unit No.11**	Turns on when unit No. 11 is in the RUN mode. Turns off when unit No. 11 is in the PROG. mode.
R909B		**Unit No.12**	Turns on when unit No. 12 is in the RUN mode. Turns off when unit No. 12 is in the PROG. mode.
R909C		**Unit No.13**	Turns on when unit No. 13 is in the RUN mode. Turns off when unit No. 13 is in the PROG. mode.
R909D		**Unit No.14**	Turns on when unit No. 14 is in the RUN mode. Turns off when unit No. 14 is in the PROG. mode.
R909E		**Unit No.15**	Turns on when unit No. 15 is in the RUN mode. Turns off when unit No. 15 is in the PROG. mode.
R909F		**Unit No.16**	Turns on when unit No. 16 is in the RUN mode. Turns off when unit No. 16 is in the PROG. mode.

Note) When the system registers 46=K0, PC link 0 for the link unit with a smaller slot No. and PC link 1 for one with a larger slot No.
When the system registers 46=K1, PC link 1 for the link unit with a smaller slot No. and PC link 0 for one with a larger slot No.

FP2/FP2SH/FP10SH

Address	Name	Description
R9100	**IC memory card installation flag (Available PLC: FP2SH/ FP10SH)**	Monitors whether the IC memory card is installed or not: - on: IC memory card is installed. - off: IC memory card is not installed.
R9101 (*Note)	**IC memory card backup battery flag 1 (Available PLC: FP2SH/ FP10SH)**	Monitors the voltage drop condition for the IC memory card as: - on: Data in the IC memory card cannot be guaranteed. - off: Data in the IC memory card can be maintained.
R9102 (*Note)	**IC memory card backup battery flag 2 (Available PLC: FP2SH/ FP10SH)**	Monitors the voltage drop condition for the IC memory card as: FP2SH: - on: Battery charge or replacement is required. - off: Battery charge or replacement is not required. FP10SH: - on: Battery replacement is required. - off: Battery replacement is not required.
R9103	**IC memory card protect switch flag (Available PLC: FP2SH/ FP10SH)**	Monitors the protective condition of the IC memory card as: - on: The protect switch is not in the write-protected (WP) position. - off: The protect switch is in the write-protected (WP) position.
R9104	**IC memory card access switch flag (Available PLC: FP2SH/ FP10SH)**	Monitors the condition of the IC memory card access enables switch as: - on (access enabled): The access enable switch is in the on position. – off (access disabled): The access enable switch is in the off position.
R9105 to R910F	**Not used**	-

Note) The IC memory card backup battery condition can be judged using special internal relays R9101 and R9102 as follows:

R9101	R9102	IC memory card condition
OFF	**OFF**	Not battery charge (replacement) required.
ON	**OFF**	Charge (replace) backup battery. The data in the IC memory card is maintained.
ON	**ON**	The data in the IC memory card cannot be maintained. Charge (replace) backup battery.

11.1.3 Special Data Registers for FP2/FP2SH/FP10SH/FP3

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-ing</th><th rowspan="2">Writ-ing</th></tr>
<tr><th>FP3</th><th>FP2/ FP2SH FP10SH</th></tr>
<tr><td>DT9000</td><td>DT90000</td><td>Self-diagnostic error code</td><td>The self-diagnostic error code is stored here when a self-diagnostic error occurs. Monitor the error code using decimal display.</td><td>A</td><td>N/A</td></tr>
<tr><td>DT9001</td><td>DT90001</td><td>Not used</td><td>-</td><td>N/A</td><td>N/A</td></tr>
<tr><td rowspan="2">DT9002</td><td rowspan="2">DT90002</td><td>Communication error of MEWNET-TR master unit (slot No. 0 to 15) (Available PLC: FP3/FP10SH)</td><td rowspan="4">The slot number, where an erroneous unit is installed, can be monitored here. “1” (on) is set in the bit position corresponding to the slot number when one of the errors below id detected.
Communication error MEWNET-TR master unit
When a communication error occurs at the MEWNET-TR master unit, the bit corresponding to the slot no. of the unit will be set on “1”. Monitor using binary display.
(1: erroneous MEWNET-TR master unit, 0: normal)
Position of abnormal I/O slot
When an error occurs at an I/O unit, the bit corresponding to the slot of the unit will be set on “1”. Monitor using binary display.
(1: error, 0: normal)
<table><tr><td>Bit position</td><td>15 . . 21</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slot No.</td><td>15 . . 21</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>DT9002/DT90002</td><td></td><td></td><td></td><td></td></tr></table><table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slot No.</td><td>31 . . 28</td><td>27 . . 24</td><td>23 . . 20</td><td>19 . . 16</td></tr><tr><td>DT9003/DT90003</td><td></td><td></td><td></td><td></td></tr></table></td><td rowspan="4">A</td><td rowspan="4">N/A</td></tr>
<tr><td>Position of abnormal I/O slot (slot No. 0 to 15) (Available PLC: FP2/FP2SH)</td></tr>
<tr><td rowspan="2">DT9003</td><td rowspan="2">DT90003</td><td>Communication error of MEWNET-TR master unit (slot No. 16 to 31) (Available PLC: FP3/FP10SH)</td></tr>
<tr><td>Position of abnormal I/O slot (slot No. 16 to 31) (Available PLC: FP2/FP2SH)</td></tr>
</table>

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Read-ing	Writ-ing
FP3	**FP2/ FP2SH FP10SH**				
DT9006	**DT90006**	**Abnormal intelligent unit (slot No. 0 to 15)**	When an error condition is detected in an intelligent unit, the bit corresponding to the slot of the unit will be set to on. Monitor using binary display. (1: abnormal intelligent unit, 0: normal intelligent unit) Bit position: 15 . . 21 | 11 . . 8 | 7 . . 4 | 3 . . 0 Slot No.: 15 . . 21 | 11 . . 8 | 7 . . 4 | 3 . . 0 DT9006/DT90006 Bit position: 15 . . 12 | 11 . . 8 | 7 . . 4 | 3 . . 0 Slot No.: 31 . . 28 | 27 . . 24 | 23 . . 20 | 19 . . 16 DT9007/DT90007	A	N/A
DT9007	**DT90007**	**Abnormal intelligent unit (slot No. 16 to 31)**			
DT9010	**DT90010**	**I/O verify error unit (slot No. 0 to 15)**	When the state of installation of an I/O unit has changed since the power was turned on, the bit corresponding to the slot of the unit will be set to on. Monitor using binary display. (1: error, 0: normal) Bit position: 15 . . 21 | 11 . . 8 | 7 . . 4 | 3 . . 0 Slot No.: 15 . . 21 | 11 . . 8 | 7 . . 4 | 3 . . 0 DT9010/DT90010 Bit position: 15 . . 12 | 11 . . 8 | 7 . . 4 | 3 . . 0 Slot No.: 31 . . 28 | 27 . . 24 | 23 . . 20 | 19 . . 16 DT9011/DT90011		
DT9011	**DT90011**	**I/O verify error unit (slot No. 16 to 31)**			
DT9014	**DT90014**	**Auxiliary register for operation**	One shift-out hexadecimal digit is stored in bit positions 0 to 3 when F105 (BSR)/P105 (PBSR) or f106 (BSL)/P106 (PBSL) instruction is executed.		
DT9015	**DT90015**	**Auxiliary register for operation**	The divided remainder (16-bit) is stored in DT9015/DT90015 when F32 (%)/P32 (P%) or F52(B%)/P52 (PB%) instruction is executed. The divided remainder (32-bit) is stored in DT9015 and DT9016/DT90015 and DT90016 when F33 (D%)/P33 (PD%) or F53(DB%)/P53 (PDB%) instruction is executed.		
DT9016	**DT90016**				
DT9017	**DT90017**	**Operation error address (hold)**	After commencing operation, the address where the first operation error occurred is stored. Monitor the address using decimal display. FP2SH: When the higher byte of DT90257 is H2, the error occurs in the 2nd program block. In case of the 1st program block, it is H1.		

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Reading	Writing
FP3	FP2/ FP2SH FP10SH				
DT9018	**DT90018**	**Operation error address (non-hold)**	The address where an operation error occurred is stored. Each time an error occurs, the new address overwrites the previous address. At the beginning of scan, the addresses 0. Monitor the address using decimal display. FP2SH: When the higher byte of DT90257 is H2, the error occurs in the 2nd program block. In case of the 1st program block, it is H1.	A	N/A
DT9019	**DT90019**	**2.5 ms ring counter**	The data stored here is increased by one every 2.5 ms (H0 to HFFFF) Difference between the values of the two points (absolute value) x 2.5 ms = Elapsed time between the two points.		
DT9020	**-**	**Maximum value of program (Available PLC: FP3)**	The last address of sequence program area set in system register 0 is stored.	N/A	N/A
-	**DT90020**	**Display of program capacity (Available PLC: FP10SH)**	The program capacity is stored in decimal. **Example:** K30: approx. 30 K steps K60: approx. 60 K steps (with memory expansion)		
		Display of program capacity (Available PLC: FP2)	The program capacity is stored in decimal. **Example:** K16: approx. 16 K steps (K15870) K32: approx. 32 K steps (with memory expansion)		
DT9021 (*Note)	**-**	**Maximum value of file register (Available PLC: FP3)**	The maximum (last) address of the file registers available are stored in here.		
-	**DT90021 (*Note)**	**Maximum value of file register (Available PLC: FP2/FP10SH)**	The maximum (last) address of the file registers available are stored in here.		

Note) Used by the system.

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2" colspan="2">Descriptions</th><th rowspan="2">Read-ing</th><th rowspan="2">Writ-ing</th></tr>
<tr><th>FP3</th><th>FP2/
FP2SH
FP10SH</th></tr>
<tr><td>DT9022</td><td>DT90022</td><td>Scan time (current value)</td><td>The current scan time is stored here. Scan time is calculated using the formula:
Scan time (ms) = stored data (decimal) x 0.1
Example:
K50 indicates 5 ms.</td><td rowspan="3">Scan time display is only possible in RUN mode, and shows the operation cycle time. The maximum and minimum values are cleared when each the mode is switched between RUN mode and PROG. mode.</td><td rowspan="6">A</td><td rowspan="6">N/A</td></tr>
<tr><td>DT9023</td><td>DT90023</td><td>Scan time (minimum value)</td><td>The minimum scan time is stored here. Scan time is calculated using the formula:
Scan time (ms) = stored data (decimal) x 0.1
Example:
K50 indicates 5 ms.</td></tr>
<tr><td>DT9024</td><td>DT90024</td><td>Scan time (maximum value)</td><td>The maximum scan time is stored here. Scan time is calculated using the formula:
Scan time (ms) = stored data (decimal) x 0.1
Example:
K125 indicates 12.5 ms.</td></tr>
<tr><td>DT9025 (*Note)</td><td>DT90025</td><td>Mask condition monitoring register for interrupt unit initiated interrupts (INT 0 to 15) (*FP2: Not used)</td><td colspan="2">The mask conditions of interrupt unit initiated interrupts using ICTL instruction can be monitored here. Monitor using binary display.
<table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>INT program</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>DT9025/DT90025</td><td></td><td></td><td></td><td></td></tr></table>0: interrupt disabled (masked)
1: interrupt enabled (unmasked)</td></tr>
<tr><td>DT9026 (*Note)</td><td>DT90026</td><td>Mask condition monitoring register for interrupt unit initiated interrupts (INT 16 to 23) (*FP2: Not used)</td><td colspan="2">The mask conditions of interrupt unit initiated interrupts using ICTL instruction can be monitored here. Monitor using binary display.
<table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>INT program</td><td>———</td><td>———</td><td>23 . . 20</td><td>19 . . 16</td></tr><tr><td>DT9026/DT90026</td><td></td><td></td><td></td><td></td></tr></table>0: interrupt disabled (masked)
1: interrupt enabled (unmasked)</td></tr>
<tr><td>DT9027 (*Note)</td><td>DT90027</td><td>Periodical interrupt interval (INT24)</td><td colspan="2">The value set by ICTL instruction is stored.
K0: periodical interrupt is not used.
K1 to K3000: 10ms to 30s or 0.5ms to 1.5s</td></tr>
</table>

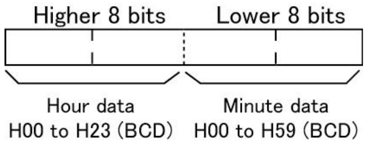
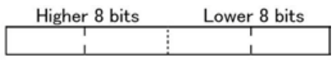
Note) Used by the system.

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-ing</th><th rowspan="2">Writ-ing</th></tr>
<tr><th>FP3</th><th>FP2/ FP2SH FP10SH</th></tr>
<tr><td>DT9028 (*Note)</td><td>DT90028</td><td>Sample trace interval</td><td>The value registered using programming tool software is stored.
- K0: sampling triggered by F155 (SMPL)/P155 (PSMPL) instruction
- K1 to K3000 (x 10ms): 10ms to 30s</td><td rowspan="8">A</td><td rowspan="8">N/A</td></tr>
<tr><td>DT9029 (*Note)</td><td>DT90029</td><td>Break address</td><td>The address (K constant) of a break in a test run is stored.</td></tr>
<tr><td>DT9030 (*Note)</td><td>DT90030</td><td>Message 0</td><td rowspan="6">The contents of the specified message are stored in these special data registers when F149 (MSG)/P149 (PMSG) instruction is executed.</td></tr>
<tr><td>DT9031 (*Note)</td><td>DT90031</td><td>Message 1</td></tr>
<tr><td>DT9032 (*Note)</td><td>DT90032</td><td>Message 2</td></tr>
<tr><td>DT9033 (*Note)</td><td>DT90033</td><td>Message 3</td></tr>
<tr><td>DT9034 (*Note)</td><td>DT90034</td><td>Message 4</td></tr>
<tr><td>DT9035 (*Note)</td><td>DT90035</td><td>Message 5</td></tr>
<tr><td rowspan="2">DT9036</td><td rowspan="2">DT90036</td><td>F152 (RMRD)/ P152 (PRMRD) and F153 (RMWT)/ P153 (PRMWT) instructions end code</td><td>The error code is stored here if F152 (RMRD)/P152 (PRMRD) or F153 (RMWT)/P153 (PRMWT) instruction was executed abnormally.
When the instruction was successfully executed, “0” is stored.</td><td rowspan="2">A</td><td rowspan="2">N/A</td></tr>
<tr><td>Abnormal unit display</td><td>If an abnormal unit is installed to the backplane, the slot number of that unit will be stored. Monitor using decimal display.</td></tr>
<tr><td>DT9037</td><td>DT90037</td><td>Work 1 for F96 (SRC)/ P96 (PSRC) instructions</td><td>The number of data that match the searched data is stored here when F96 (SRC)/P96 (PSRC) instruction is executed.</td><td rowspan="2">A</td><td rowspan="2">A</td></tr>
<tr><td>DT9038</td><td>DT90038</td><td>Work 2 for F96 (SRC)/ P96 (PSRC) instructions</td><td>The position of the first matching data, counting from the starting 16-bit area, is stored here when an F96 (SRC)/P96 (PSRC) instruction is executed.</td></tr>
<tr><td>DT9039</td><td>DT90039</td><td>F145 (SEND)/ P145 (PSEND) and F146 (RECV)/ P146 (PRECV) instructions end code</td><td>The error code is stored here if F145 (SEND)/P145 (PSEND) or F146 (RECV)/ P146 (PRECV) instruction was executed abnormally.
When the instruction was successfully executed, “0” is stored.</td><td>A</td><td>N/A</td></tr>
</table>

Note) Used by the system.

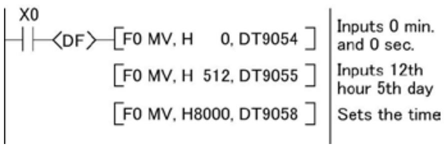
FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-ing</th><th rowspan="2">Writ-ing</th></tr>
<tr><th>FP3</th><th>FP2/ FP2SH FP10SH</th></tr>
<tr><td>DT9053</td><td>DT90053</td><td>Real-Time Clock (Clock/Calendar) monitor (hour/minute)</td><td>Hour and minute data of the Real-Time Clock(Clock/Calendar) are stored here. This data is read-only data. It cannot be overwritten.

</td><td>A</td><td>N/A</td></tr>
<tr><td>DT9054</td><td>DT90054</td><td>Real-Time Clock (Clock/Calendar) monitor and setting (minute/second)</td><td rowspan="4">The year, month, day, hour, minute, second and day-of-the-week data for the calendar timer is stored. The built-in Real-Time Clock(Clock/Calendar) will operate correctly through the year 2099 and supports leap years.
The Real-Time Clock (Clock/Calendar) can be set (the time set) by writing a value using a programming tool software or a program that uses the F0 (MV) transfer instruction.


<table><tr><td>DT9054/ DT90054</td><td>Minute data H00 to H59 (BCD)</td><td>Second data H00 to H59 (BCD)</td></tr><tr><td>DT9055/ DT90055</td><td>Day data H01 to H31 (BCD)</td><td>Hour data H00 to H23 (BCD)</td></tr><tr><td>DT9056/ DT90056</td><td>Year data H00 to H99 (BCD)</td><td>Month data H01 to H12 (BCD)</td></tr><tr><td>DT9057/ DT90057</td><td>—</td><td>Day-of-the-week data H00 to H06 (BCD)</td></tr></table></td><td rowspan="4">A</td><td rowspan="4">A</td></tr>
<tr><td>DT9055</td><td>DT90055</td><td>Real-Time Clock (Clock/Calendar) monitor and setting (day/hour)</td></tr>
<tr><td>DT9056</td><td>DT90056</td><td>Real-Time Clock (Clock/Calendar) monitor and setting (year/month)</td></tr>
<tr><td>DT9057</td><td>DT90057</td><td>Real-Time Clock (Clock/Calendar) monitor and setting (day-of-the-week)</td></tr>
</table>

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-
ing</th><th rowspan="2">Writ-
ing</th></tr>
<tr><th>FP3</th><th>FP2/
FP2SH
FP10SH</th></tr>
<tr><td>DT9058</td><td>DT90058</td><td>Real-Time Clock (Clock /Calendar) setting and 30 seconds correction</td><td>The Real-Time Clock(Clock/Calendar) is adjusted as follows.
When setting the Real-Time Clock (Clock/Calendar) by program
By setting the highest bit of DT9058/DT90058 to 1, the time becomes that written to DT9054 to DT9057/DT90054 to DT90057 by F0 (MV) instruction. After the time is set, DT9058/DT90058 is cleared to 0. (Cannot be performed with any instruction other than F0 (MV) instruction.)

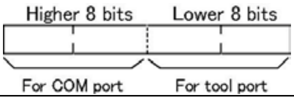
<Example>
Set the time to 12:00:00 on the 5th day when the X0 turns on.

If you changed the values of DT9054 to DT9057/DT90054 to DT90057 with programming tool software, the time will be set when the new values are written. Therefore, it is unnecessary to write to DT9058/DT90058.

When the correcting times less than 30 seconds-
By setting the lowest bit of DT9058/DT90058 to 1, the value will be moved up or down and become exactly 0 seconds. After the correction is completed, DT9058/DT90058 is cleared to 0.

<Example>
Correct to 0 seconds with X0 turns on.

At the time of correction, if between 0 and 29 seconds, it will be moved down, and if the between 30 and 59 seconds, it will be moved up. In the example above, if the time was 5 minutes 29 seconds, it will become 5 minutes 0 second; and, if the time was 5 minutes 35 seconds, it will become 6 minutes 0 second.</td><td>A</td><td>A</td></tr>
</table>

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-ing</th><th rowspan="2">Writ-ing</th></tr>
<tr><th>FP3</th><th>FP2/ FP2SH FP10SH</th></tr>
<tr><td>DT9059 (*Note)</td><td>DT90059</td><td>Serial communication error code</td><td>The system uses this as a communication status when communication error occurs.

</td><td>A</td><td>N/A</td></tr>
<tr><td>DT9060</td><td>DT90060</td><td>Step ladder process (0 to 15)</td><td rowspan="18">Indicates the startup condition of the step ladder process. When the process starts up, the bit corresponding to the process number turns on “1”.

Monitor using binary display.

(0: not-executing, 1: executing)

Example:
<table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Process number</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>DT9060/DT90060</td><td>0 0 0 0</td><td>0 0 0 0</td><td>0 0 0 0</td><td>0 0 0 1</td></tr></table>
Since bit position 0 of DT9060/DT90060 is “1”, step ladder process 0 is executing.

A programming tool software can be used to write data.</td><td rowspan="18">A</td><td rowspan="18">A</td></tr>
<tr><td>DT9061</td><td>DT90061</td><td>Step ladder process (16 to 31)</td></tr>
<tr><td>DT9062</td><td>DT90062</td><td>Step ladder process (32 to 47)</td></tr>
<tr><td>DT9063</td><td>DT90063</td><td>Step ladder process (48 to 63)</td></tr>
<tr><td>DT9064</td><td>DT90064</td><td>Step ladder process (64 to 79)</td></tr>
<tr><td>DT9065</td><td>DT90065</td><td>Step ladder process (80 to 95)</td></tr>
<tr><td>DT9066</td><td>DT90066</td><td>Step ladder pro-cess (96 to 111)</td></tr>
<tr><td>DT9067</td><td>DT90067</td><td>Step ladder pro-cess (112 to 127)</td></tr>
<tr><td>DT9068</td><td>DT90068</td><td>Step ladder pro-cess (128 to 143)</td></tr>
<tr><td>DT9069</td><td>DT90069</td><td>Step ladder pro-cess (144 to 159)</td></tr>
<tr><td>DT9070</td><td>DT90070</td><td>Step ladder pro-cess (160 to 175)</td></tr>
<tr><td>DT9071</td><td>DT90071</td><td>Step ladder pro-cess (176 to 191)</td></tr>
<tr><td>DT9072</td><td>DT90072</td><td>Step ladder pro-cess (192 to 207)</td></tr>
<tr><td>DT9073</td><td>DT90073</td><td>Step ladder pro-cess (208 to 223)</td></tr>
<tr><td>DT9074</td><td>DT90074</td><td>Step ladder pro-cess (224 to 239)</td></tr>
<tr><td>DT9075</td><td>DT90075</td><td>Step ladder pro-cess (240 to 255)</td></tr>
<tr><td>DT9076</td><td>DT90076</td><td>Step ladder pro-cess (256 to 271)</td></tr>
<tr><td>DT9077</td><td>DT90077</td><td>Step ladder pro-cess (272 to 287)</td></tr>
</table>

Note) Used by the system.

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-
ing</th><th rowspan="2">Writ-
ing</th></tr>
<tr><th>FP3</th><th>FP2/
FP2SH
FP10SH</th></tr>
<tr><td>DT9078</td><td>DT90078</td><td>Step ladder process (288 to 303)</td><td rowspan="22">Indicates the startup condition of the step ladder process. When the process starts up, the bit corresponding to the process number turns on “1”.

Monitor using binary display.

(0: not-executing, 1: executing)

Example:
<table><tr><td>Bit position</td><td colspan="4">15 . . 12</td><td colspan="4">11 . . 8</td><td colspan="4">7 . . 4</td><td colspan="4">3 . . 0</td></tr><tr><td>Process number</td><td colspan="4">335 . 332</td><td colspan="4">331 . 328</td><td colspan="4">327. 324</td><td colspan="4">323 . 320</td></tr><tr><td>DT9080/DT90080</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></table>
Since bit position 0 of DT9080/DT90080 is “1”, step ladder process 320 is executing.

A programming tool software can be used to write data.</td><td rowspan="22">A</td><td rowspan="22">A</td></tr>
<tr><td>DT9079</td><td>DT90079</td><td>Step ladder process (304 to 319)</td></tr>
<tr><td>DT9080</td><td>DT90080</td><td>Step ladder process (320 to 335)</td></tr>
<tr><td>DT9081</td><td>DT90081</td><td>Step ladder process (336 to 351)</td></tr>
<tr><td>DT9082</td><td>DT90082</td><td>Step ladder process (352 to 367)</td></tr>
<tr><td>DT9083</td><td>DT90083</td><td>Step ladder process (368 to 383)</td></tr>
<tr><td>DT9084</td><td>DT90084</td><td>Step ladder process (384 to 399)</td></tr>
<tr><td>DT9085</td><td>DT90085</td><td>Step ladder process (400 to 415)</td></tr>
<tr><td>DT9086</td><td>DT90086</td><td>Step ladder process (416 to 431)</td></tr>
<tr><td>DT9087</td><td>DT90087</td><td>Step ladder process (432 to 447)</td></tr>
<tr><td>DT9088</td><td>DT90088</td><td>Step ladder process (448 to 463)</td></tr>
<tr><td>DT9089</td><td>DT90089</td><td>Step ladder process (464 to 479)</td></tr>
<tr><td>DT9090</td><td>DT90090</td><td>Step ladder process (480 to 495)</td></tr>
<tr><td>DT9091</td><td>DT90091</td><td>Step ladder process (496 to 511)</td></tr>
<tr><td>DT9092</td><td>DT90092</td><td>Step ladder process (512 to 527)</td></tr>
<tr><td>DT9093</td><td>DT90093</td><td>Step ladder process (528 to 543)</td></tr>
<tr><td>DT9094</td><td>DT90094</td><td>Step ladder process (544 to 559)</td></tr>
<tr><td>DT9095</td><td>DT90095</td><td>Step ladder process (560 to 575)</td></tr>
<tr><td>DT9096</td><td>DT90096</td><td>Step ladder process (576 to 591)</td></tr>
<tr><td>DT9097</td><td>DT90097</td><td>Step ladder process (592 to 607)</td></tr>
<tr><td>DT9098</td><td>DT90098</td><td>Step ladder process (608 to 623)</td></tr>
<tr><td>DT9099</td><td>DT90099</td><td>Step ladder process (624 to 639)</td></tr>
</table>

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-ing</th><th rowspan="2">Writ-ing</th></tr>
<tr><th>FP3</th><th>FP2/ FP2SH FP10SH</th></tr>
<tr><td>DT9100</td><td>DT90100</td><td>Step ladder process (640 to 655)</td><td rowspan="23">Indicates the startup condition of the step ladder process. When the process starts up, the bit corresponding to the process number turns on “1”.

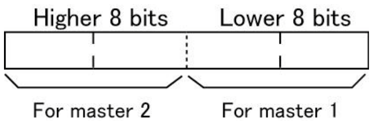
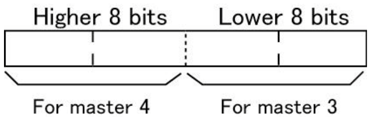
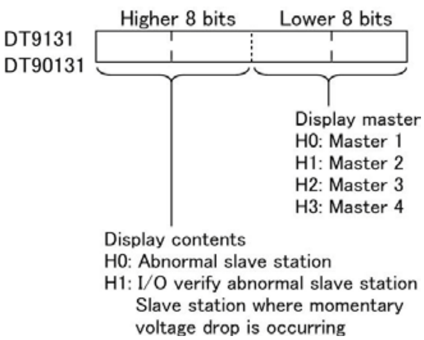
Monitor using binary display.

(0: not-executing, 1: executing)

Example:
<table>
<tr><td>Bit position</td><td colspan="4">15 . . 12</td><td colspan="4">11 . . 8</td><td colspan="4">7 . . 4</td><td colspan="4">3 . . 0</td></tr>
<tr><td>Process number</td><td colspan="4">655 . 652</td><td colspan="4">651 . 648</td><td colspan="4">647. 644</td><td colspan="4">643 . 640</td></tr>
<tr><td>DT9100/DT90100</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
</table>
Since bit position 0 of DT9100/DT90100 is “1”, step ladder process 640 is executing.

A programming tool software can be used to write data.</td><td rowspan="23">A</td><td rowspan="23">A</td></tr>
<tr><td>DT9101</td><td>DT90101</td><td>Step ladder process (656 to 671)</td></tr>
<tr><td>DT9102</td><td>DT90102</td><td>Step ladder process (672 to 687)</td></tr>
<tr><td>DT9103</td><td>DT90103</td><td>Step ladder process (688 to 703)</td></tr>
<tr><td>DT9104</td><td>DT90104</td><td>Step ladder process (704 to 719)</td></tr>
<tr><td>DT9105</td><td>DT90105</td><td>Step ladder process (720 to 735)</td></tr>
<tr><td>DT9106</td><td>DT90106</td><td>Step ladder process (736 to 751)</td></tr>
<tr><td>DT9107</td><td>DT90107</td><td>Step ladder process (752 to 767)</td></tr>
<tr><td>DT9108</td><td>DT90108</td><td>Step ladder process (768 to 783)</td></tr>
<tr><td>DT9109</td><td>DT90109</td><td>Step ladder process (784 to 799)</td></tr>
<tr><td>DT9110</td><td>DT90110</td><td>Step ladder process (800 to 815)</td></tr>
<tr><td>DT9111</td><td>DT90111</td><td>Step ladder process (816 to 831)</td></tr>
<tr><td>DT9112</td><td>DT90112</td><td>Step ladder process (832 to 847)</td></tr>
<tr><td>DT9113</td><td>DT90113</td><td>Step ladder process (848 to 863)</td></tr>
<tr><td>DT9114</td><td>DT90114</td><td>Step ladder process (864 to 879)</td></tr>
<tr><td>DT9115</td><td>DT90115</td><td>Step ladder process (880 to 895)</td></tr>
<tr><td>DT9116</td><td>DT90116</td><td>Step ladder process (896 to 911)</td></tr>
<tr><td>DT9117</td><td>DT90117</td><td>Step ladder process (912 to 927)</td></tr>
<tr><td>DT9118</td><td>DT90118</td><td>Step ladder process (928 to 943)</td></tr>
<tr><td>DT9119</td><td>DT90119</td><td>Step ladder process (944 to 959)</td></tr>
<tr><td>DT9120</td><td>DT90120</td><td>Step ladder process (960 to 975)</td></tr>
<tr><td>DT9121</td><td>DT90121</td><td>Step ladder process (976 to 991)</td></tr>
<tr><td>DT9122</td><td>DT90122</td><td>Step ladder process (992 to 999) (higher byte is not used.)</td></tr>
</table>

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

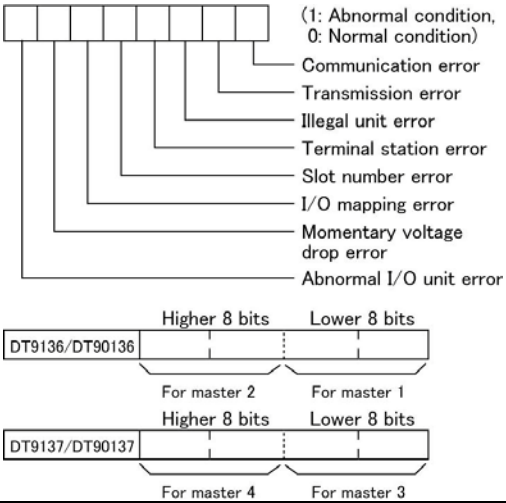
Address		Name	Descriptions	Read-ing	Writ-ing
FP3	FP2/ FP2SH FP10SH				
DT9123	**DT90123**	**Not used**	-	N/A	N/A
DT9124	**DT90124**	**Not used**	-		
DT9125	**DT90125**	**Not used**	-		
DT9126 (*Note)	**DT90126**	**Forced on/off operating station display**	This displays the unit number that has executed forced on/off operation.	A	N/A
DT9127 (*Note)	**DT90127**	**MEWNET-F system remote I/O service time**	The number of times, which MEWNET-F remote I/O service was performed by each master, is stored. 		
DT9128 (*Note)	**DT90128**		The number of times, which MEWNET-F remote I/O service was performed by each master, is stored. 		
DT9129	**DT90129**	**Not used**	-	N/A	N/A
DT9130	**DT90130**	**Not used**	-		
DT9131	**DT90131**	**MEWNET-F (remote I/O) slave stations abnormality checking (for selecting the display contents and master of DT9132 to DT9135/DT90132 to DT90135)**	The contents displayed by DT9132 to DT9135/DT90132 to DT90135 will change depending on the contents of stored in DT9131/DT90131. Use the programming tools software to write the settings for what you want to display (this can also be done with the F0 (MV) move instruction). Set the code (H0 or H1) specifying the display contents in the higher 8 bits and set the code (H0 to H3) specifying the display master in the lower 8 bits. 	A	N/A

Note) Used by the system.

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-
ing</th><th rowspan="2">Writ-
ing</th></tr>
<tr><th>FP3</th><th>FP2/
FP2SH
FP10SH</th></tr>
<tr><td rowspan="2">DT9132
DT9133</td><td rowspan="2">DT90132
DT90133</td><td>MEWNET-F (remote I/O) error slave station number – current condition (when DT9131/ DT90131 is H0, H1, H2 or H3)</td><td>The bit corresponding to the station number of the MEWNET-F where an error is occurring is set to on. Monitor using binary display.
(1: Error slave station, 0: Normal slave station)<table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slave station no.</td><td>16 . . 13</td><td>12 . . 9</td><td>8 . . 5</td><td>4 . . 1</td></tr><tr><td>DT9132/DT90132</td><td></td><td></td><td></td><td></td></tr></table><table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slave station no.</td><td>32 . . 29</td><td>28 . . 25</td><td>24 . . 21</td><td>20 . . 17</td></tr><tr><td>DT9133/DT90133</td><td></td><td></td><td></td><td></td></tr></table></td><td rowspan="4">A</td><td rowspan="4">N/A</td></tr>
<tr><td>MEWNET-F (remote I/O) I/O verify error slave station number (when DT9131/ DT90131 is H100, H101, H102 or H103)</td><td>When the installed condition of a MEWNET-F slave station set unit has changed since the power was turned on, the bit corresponding to that slave station number will be set to on. Monitor using binary display.
(1: Error slave station, 0: Normal slave station)<table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slave station no.</td><td>16 . . 13</td><td>12 . . 9</td><td>8 . . 5</td><td>4 . . 1</td></tr><tr><td>DT9132/DT90132</td><td></td><td></td><td></td><td></td></tr></table><table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slave station no.</td><td>32 . . 29</td><td>28 . . 25</td><td>24 . . 21</td><td>20 . . 17</td></tr><tr><td>DT9133/DT90133</td><td></td><td></td><td></td><td></td></tr></table></td></tr>
<tr><td rowspan="2">DT9134
DT9135</td><td rowspan="2">DT90134
DT90135</td><td>MEWNET-F (remote I/O) error slave station number – record (when DT9131/ DT90131 is H0, H1, H2 or H3)</td><td>The bit corresponding to the slave station number of the MEWNET-F where an error is occurring will be set to on. Monitor using binary display.
(1: Error slave station, 0: Normal slave station)<table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slave station no.</td><td>16 . . 13</td><td>12 . . 9</td><td>8 . . 5</td><td>4 . . 1</td></tr><tr><td>DT9134/DT90134</td><td></td><td></td><td></td><td></td></tr></table><table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slave station no.</td><td>32 . . 29</td><td>28 . . 25</td><td>24 . . 21</td><td>20 . . 17</td></tr><tr><td>DT9135/DT90135</td><td></td><td></td><td></td><td></td></tr></table></td></tr>
<tr><td>MEWNET-F (remote I/O) momentary voltage drop slave station number (when DT9131/ DT90131 is H100, H101, H102 or H103)</td><td>If a momentary voltage drop at MEWNET-F slave station set, the bit corresponding to that slave station number will be set to on. Monitor using binary display.
(1: Error slave station, 0: Normal slave station)<table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slave station no.</td><td>16 . . 13</td><td>12 . . 9</td><td>8 . . 5</td><td>4 . . 1</td></tr><tr><td>DT9134/DT90134</td><td></td><td></td><td></td><td></td></tr></table><table><tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr><tr><td>Slave station no.</td><td>32 . . 29</td><td>28 . . 25</td><td>24 . . 21</td><td>20 . . 17</td></tr><tr><td>DT9135/DT90135</td><td></td><td></td><td></td><td></td></tr></table></td></tr>
</table>

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Read-ing	Writ-ing
FP3	**FP2/ FP2SH FP10SH**				
DT9136 DT9137	**DT90136 DT90137**	**Error code of MEWNET-F (remote I/O) system**	Display the error conditions for 8 types of errors using 1 byte.  	A	N/A
DT9138	**DT90138**	**Not used**	-	N/A	N/A
DT9139	**DT90139**	**Not used**	-		
DT9140	**DT90140**	**MEWNET-W/-P PC(PLC) link status [PC(PLC) link 0 (W/P)] (*Note2, 3)**	The number of times the receiving operation is performed (counted using ring counter)	N/A	N/A
DT9141 (*Note1)	**DT90141**		The current interval between two receiving operations: value in the register x 2.5 ms		
DT9142 (*Note1)	**DT90142**		The minimum interval between two receiving operations: value in the register x 2.5 ms		
DT9143 (*Note1)	**DT90143**		The maximum interval between two receiving operations: value in the register x 2.5 ms		
DT9144 (*Note1)	**DT90144**		The number of times the sending operation is performed (counted using ring counter)		
DT9145 (*Note1)	**DT90145**		The current interval between two sending operations: value in the register x 2.5 ms		
DT9146 (*Note1)	**DT90146**		The minimum interval between two sending operations: value in the register x 2.5 ms		
DT9147 (*Note1)	**DT90147**		The maximum interval between two sending operations: value in the register x 2.5 ms		

Note1) Used by the system.

Note2) When the system register 46 = K0, First: PC(PLC) link 0, second: PC(PLC) link 1
When the system register 46 = K1, First: PC(PLC) link 1, second: PC(PLC) link 0

Note3) For MEWNET-W system, available PLC type: FP2/FP2SH/FP3/FP10SH
For MEWNET-P system, available PLC type: FP3/FP10SH

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Reading	Writing
FP3	**FP2/ FP2SH FP10SH**				
DT9148 (*Note1)	**DT90148**	**MEWNET-W/-P PC(PLC) link status [PC(PLC) link 1 (W/P)] (*Note2, 3)**	The number of times the receiving operation is performed (counted using ring counter)	N/A	N/A
DT9149 (*Note1)	**DT90149**		The current interval between two receiving operations: value in the register x 2.5 ms		
DT9150 (*Note1)	**DT90150**		The minimum interval between two receiving operations: value in the register x 2.5 ms		
DT9151 (*Note1)	**DT90151**		The maximum interval between two receiving operations: value in the register x 2.5 ms		
DT9152 (*Note1)	**DT90152**		The number of times the sending operation is performed (counted using ring counter)		
DT9153 (*Note1)	**DT90153**		The current interval between two sending operations: value in the register x 2.5 ms		
DT9154 (*Note1)	**DT90154**		The minimum interval between two sending operations: value in the register x 2.5 ms		
DT9155 (*Note1)	**DT90155**		The maximum interval between two sending operations: value in the register x 2.5 ms		
DT9156 (*Note1)	**DT90156**	**MEWNET-W/-P PC(PLC) link status [PC(PLC) link 0 (W/P)] (*Note2, 3)**	Area used for measurement of receiving interval.		
DT9157 (*Note1)	**DT90157**		Area used for measurement of sending interval.		
DT9158 (*Note1)	**DT90158**	**MEWNET-W/-P PC(PLC) link status [PC(PLC) link 1 (W/P)] (*Note2, 3)**	Area used for measurement of receiving interval.		
DT9159 (*Note1)	**DT90159**		Area used for measurement of sending interval.		

Note1) Used by the system.

Note2) When the system register 46 = K0, First: PC(PLC) link 0, second: PC(PLC) link 1
When the system register 46 = K1, First: PC(PLC) link 1, second: PC(PLC) link 0

Note3) For MEWNET-W system, available PLC type: FP2/FP2SH/FP3/FP10SH
For MEWNET-P system, available PLC type: FP3/FP10SH

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Read-ing	Writ-ing
FP3	FP2/ FP2SH FP10SH				
DT9160	**DT90160**	**Link unit no. [W/P link 1] (*Note)**	Stores the unit No. of link 1.	A	N/A
DT9161	**DT90161**	**Error flag [W/P link 1] (*Note)**	Stores the error flag of link 1.		
DT9162	**DT90162**	**Link unit no. [W/P link 2] (*Note)**	Stores the unit No. of link 2.		
DT9163	**DT90163**	**Error flag [W/P link 2] (*Note)**	Stores the error flag of link 2.		
DT9164	**DT90164**	**Link unit no. [W/P link 3] (*Note)**	Stores the unit No. of link 3.		
DT9165	**DT90165**	**Error flag [W/P link 3] (*Note)**	Stores the error flag of link 3.		
-	**DT90166**	**Link unit no. [W/P link 4] Available PLC: FP2SH, FP10SH**	Stores the unit No. of link 4.		
-	**DT90167**	**Error flag [W/P link 4] Available PLC: FP2SH, FP10SH**	Stores the error flag of link 4.		
-	**DT90168**	**Link unit no. [W/P link 5] Available PLC: FP2SH, FP10SH**	Stores the unit No. of link 5.		
-	**DT90169**	**Error flag [W/P link 5] Available PLC: FP2SH, FP10SH**	Stores the error flag of link 5.		

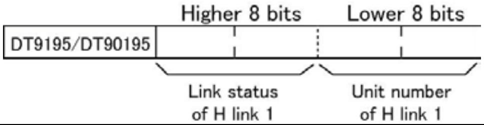
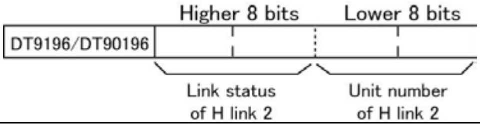
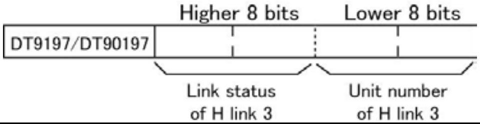
Note) For MEWNET-W system, available PLC type: FP2/FP2SH/FP3/FP10SH
For MEWNET-P system, available PLC type: FP3/FP10SH

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Read-ing	Writ-ing
FP3	FP2/ FP2SH FP10SH				
DT9170	**DT90170**	**MEWNET-W/-P link status [W/P link 1] (*Note)**	Station number, where the send area address for the PC link is overlapped with this station, is stored here.	A	N/A
DT9171	**DT90171**		Test result in the optical transmission path test mode for MEWNET-P link system is stored here.		
DT9172	**DT90172**		Counts how many times a token is lost.		
DT9173	**DT90173**		Counts how many times two or more tokens are detected.		
DT9174	**DT90174**		Counts how many times a signal is lost.		
DT9175	**DT90175**		Counts how many times a synchronous abnormality is detected.		
DT9176	**DT90176**		Send NACK		
DT9177	**DT90177**		Send NACK		
DT9178	**DT90178**		Send WACK		
DT9179	**DT90179**		Send WACK		
DT9180	**DT90180**		Send answer		
DT9181	**DT90181**		Send answer		
DT9182	**DT90182**		Unidentified command		
DT9183	**DT90183**		Counts how many times a parity error is detected.		
DT9184	**DT90184**		End code receiving error		
DT9185	**DT90185**		Format error		
DT9186	**DT90186**		Not support error		
DT9187	**DT90187**		Self-diagnostic result		
DT9188	**DT90188**		Counts how many times loop change is detected. Available PLC: FP3, FP10SH		
DT9189	**DT90189**		Counts home many times link error is detected.		
DT9190	**DT90190**		Counts how many times main loop break is detected. Available PLC: FP3, FP10SH		
DT9191	**DT90191**		Counts how many times sub loop break is detected. Available PLC: FP3, FP10SH		
DT9192	**DT90192**		Loop reconstruction condition Available PLC: FP3, FP10SH		
DT9193	**DT90193**		Loop operation mode Available PLC: FP3, FP10SH		
DT9194	**DT90194**		Loop input status Available PLC: FP3, FP10SH		

Note) For MEWNET-W system, available PLC type: FP2/FP2SH/FP3/FP10SH
For MEWNET-P system, available PLC type: FP3/FP10SH

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Read-ing	Writ-ing
FP3	FP2/ FP2SH FP10SH				
DT9195	**DT90195**	**MEWNET-H link status/ link unit number (H link 1) (*Note1)**	The link status for the MEWNET-H link is monitored as: 	A	N/A
DT9196	**DT90196**	**MEWNET-H link status/ link unit number (H link 2) (*Note1)**	The link status for the MEWNET-H link is monitored as: 		
DT9197	**DT90197**	**MEWNET-H link status/ link unit number (H link 3) (*Note1)**	The link status for the MEWNET-H link is monitored as: 		
DT9198	**DT90198**	**Not used**	-	N/A	N/A
DT9199	**DT90199**	**Not used**	-		
DT9200	**DT90200**	**MEWNET-W/-P link status [W/P link 2] (*Note2)**	Station number, where the send area address for the PC(PLC) link is overlapped with this station, is stored here.	A	N/A
DT9201	**DT90201**		Test result in the optical transmission path test mode for MEWNET-P link system is stored here.		
DT9202	**DT90202**		Counts how many times a token is lost.		
DT9203	**DT90203**		Counts how many times two or more tokens are detected.		
DT9204	**DT90204**		Counts how many times a signal is lost.		
DT9205	**DT90205**		Counts how many times a synchronous abnormality is detected.		
DT9206	**DT90206**		Send NACK		
DT9207	**DT90207**		Send NACK		
DT9208	**DT90208**		Send WACK		
DT9209	**DT90209**		Send WACK		
DT9210	**DT90210**		Send answer		
DT9211	**DT90211**		Send answer		
DT9212	**DT90212**		Unidentified command		

Note1) For FP10SH/FP3, using H mode
For FP2/FP2SH, using W2 mode
Note2) For MEWNET-W system, available PLC type: FP2/FP2SH/FP3/FP10SH
For MEWNET-P system, available PLC type: FP3/FP10SH

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Reading	Writing
FP3	FP2/ FP2SH FP10SH				
DT9213	**DT90213**	**MEWNET-W/-P link status [W/P link 2] (*Note)**	Counts how many times a parity error is detected.	A	N/A
DT9214	**DT90214**		End code receiving error		
DT9215	**DT90215**		Format error		
DT9216	**DT90216**		Not support error		
DT9217	**DT90217**		Self-diagnostic result		
DT9218	**DT90218**		Counts how many times loop change is detected. Available PLC: FP3, FP10SH		
DT9219	**DT90219**		Counts home many times link error is detected.		
DT9220	**DT90220**		Counts how many times main loop break is detected. Available PLC: FP3, FP10SH		
DT9221	**DT90221**		Counts how many times sub loop break is detected. Available PLC: FP3, FP10SH		
DT9222	**DT90222**		Loop reconstruction condition Available PLC: FP3, FP10SH		
DT9223	**DT90223**		Loop operation mode Available PLC: FP3, FP10SH		
DT9224	**DT90224**		Loop input status Available PLC: FP3, FP10SH		
DT9225	**DT90225**	**Not used**	-		
DT9226	**DT90226**	**Not used**	-		
DT9227	**DT90227**	**Not used**	-		
DT9228	**DT90228**	**Not used**	-		
DT9229	**DT90229**	**Not used**	-		
DT9230	**DT90230**	**MEWNET-W/-P link status [W/P link 3] (*Note)**	Station number, where the send area address for the PC link is overlapped with this station, is stored here.	A	N/A
DT9231	**DT90231**		Test result in the optical transmission path test mode for MEWNET-P link system is stored here.		
DT9232	**DT90232**		Counts how many times a token is lost.		
DT9233	**DT90233**		Counts how many times two or more tokens are detected.		
DT9234	**DT90234**		Counts how many times a signal is lost.		
DT9235	**DT90235**		Counts how many times a synchronous abnormality is detected.		
DT9236	**DT90236**		Send NACK		
DT9237	**DT90237**		Send NACK		

Note) For MEWNET-W system, available PLC type: FP2/FP2SH/FP3/FP10SH
For MEWNET-P system, available PLC type: FP3/FP10SH

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Read-ing	Writ-ing
FP3	FP2/ FP2SH FP10SH				
DT9238	**DT90238**	**MEWNET-W/-P link status [W/P link 3] (*Note)**	Send WACK	A	N/A
DT9239	**DT90239**		Send WACK		
DT9240	**DT90240**		Send answer		
DT9241	**DT90241**		Send answer		
DT9242	**DT90242**		Unidentified command		
DT9243	**DT90243**		Counts how many times a parity error is detected.		
DT9244	**DT90244**		End code receiving error		
DT9245	**DT90245**		Format error		
DT9246	**DT90246**		Not support error		
DT9247	**DT90247**		Self-diagnostic result		
DT9248	**DT90248**		Counts how many times loop change is detected. Available PLC: FP3, FP10SH		
DT9249	**DT90249**		Counts home many times link error is detected.		
DT9250	**DT90250**		Counts how many times main loop break is detected. Available PLC: FP3, FP10SH		
DT9251	**DT90251**		Counts how many times sub loop break is detected. Available PLC: FP3, FP10SH		
DT9252	**DT90252**		Loop reconstruction condition Available PLC: FP3, FP10SH		
DT9253	**DT90253**		Loop operation mode Available PLC: FP3, FP10SH		
DT9254	**DT90254**		Loop input status Available PLC: FP3, FP10SH		
-	**DT90255**	**Monitoring tool port station No. (Available PLC: FP2SH/ FP10SH)**	Station number BCD (H1 to H32) set for tool port is stored here.	A	N/A
-	**DT90256**	**Monitoring COM port station No. (Available PLC: FP2SH/ FP10SH)**	Station number BCD (H1 to H32) set for tool port is stored here.		

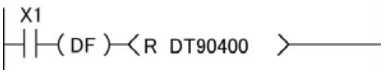
Note) For MEWNET-W system, available PLC type: FP2/FP2SH/FP3/FP10SH
For MEWNET-P system, available PLC type: FP3/FP10SH

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

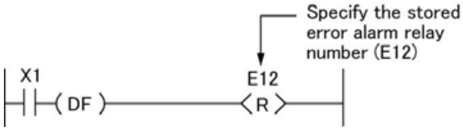
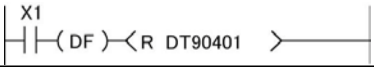
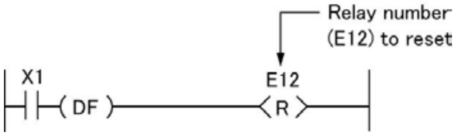
Address		Name	Descriptions	Read-ing	Writ-ing
FP3	FP2/ FP2SH FP10SH				
-	DT90257	**Operation error program No. (hold) (Available PLC: FP2SH/ FP10SH)**	An Operation error program block number is stored (higher byte) here when an operation error is detected. Program block number - H1: In the first program block - H2: In the 2nd program block	A	N/A
-	DT90258	**Operation error program No. (non-hold) (Available PLC: FP2SH/ FP10SH)**	The program block number for the latest operation error is stored here each time an operation error is detected. Program block number - H1: In the first program block - H2: In the 2nd program block		
-	DT90259	**Break occurrence program number (Available PLC: FP2SH/ FP10SH)**	The program block number where the BRK instruction occurred is stored here. Program block number - H1: In the first program block - H2: In the 2nd program block		
-	DT90260	**Type of IC memory card (Available PLC: FP2SH/ FP10SH)**	Type of IC memory card is monitored here as: - H5: Flash-EEPROM type IC memory card - H6: SRAM type IC memory card - H506: For FP10SH, flash-EEPROM/SRAM mixed type IC memory card - H6: No archival information is stored - H6: No data is written - Other than above: Erroneous condition (self-diagnostic error code E56)		
-	DT90261	**Capacity of IC memory card 1 (Available PLC: FP2SH/ FP10SH)**	The capacity of IC memory card is stored in units of KB. If Flash-EEPROM/SRAM mixed type IC memory card is used, SRAM capacity is stored.		
-	DT90262	**Capacity of IC memory card 2 (Available PLC: FP2SH/ FP10SH)**	If Flash-EEPROM/SRAM mixed type IC memory card is used, flash-EEPROM capacity is stored in units of KB.		
-	DT90263	**File register bank (current value) (Available PLC: FP2SH)**	The current value of file register bank is stored here.		

Note) For MEWNET-W system, available PLC type: FP2/FP2SH/FP3/FP10SH
For MEWNET-P system, available PLC type: FP3/FP10SH

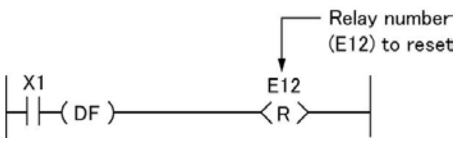
FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-
ing</th><th rowspan="2">Writ-
ing</th></tr>
<tr><th>FP3</th><th>FP2/
FP2SH
FP10SH</th></tr>
<tr><td>-</td><td>DT90264</td><td>File register bank (shelter number)
(Available PLC: FP2SH)</td><td>The shelter number of the file register bank is stored here.</td><td rowspan="3">A</td><td rowspan="3">N/A</td></tr>
<tr><td>-</td><td>DT90265</td><td>Free compile memory capacity
(Available PLC: FP2SH/ FP10SH)</td><td>Free capacity of compile memory is stored here. If the program memory is 120K steps, the capacity of 1st program block is stored.</td></tr>
<tr><td>-</td><td>DT90266</td><td>Free compile memory capacity for program block 2
(Available PLC: FP2SH/ FP10SH)</td><td>If the program memory is 120K steps, free capacity of program block 2 compile memory is stored here.</td></tr>
<tr><td>-</td><td>DT90267</td><td>Not used</td><td>-</td><td>N/A</td><td>N/A</td></tr>
<tr><td>-</td><td>DT90268</td><td>Index register bank (current value)
(Available PLC: FP2SH/ FP10SH)</td><td>The current value of index register bank is stored here.</td><td rowspan="2">A</td><td rowspan="2">A</td></tr>
<tr><td>-</td><td>DT90269</td><td>Index register bank (shelter number)
(Available PLC: FP2SH/ FP10SH)</td><td>The shelter number of index register bank is stored here.</td></tr>
<tr><td>-</td><td>DT90399</td><td>Not used</td><td>-</td><td>N/A</td><td>N/A</td></tr>
<tr><td>-</td><td>DT90400</td><td>Number of the error alarm relay which went on
(Available PLC: FP2SH/ FP10SH)</td><td>The total of the error alarm relay which went on is stored here. (Max. 500)
To reset all data in the error alarm buffer, use an RST instruction and DT90400.
</td><td>A</td><td>N/A</td></tr>
</table>

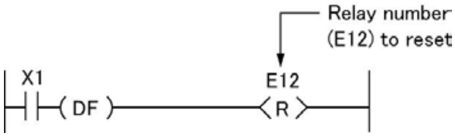
FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Reading	Writing
FP3	FP2/ FP2SH FP10SH				
-	DT90401	**First error alarm relay which went on (Available PLC: FP2SH/ FP10SH)**	The first error alarm relay number which went on is stored. The error has been reset by executing a RST instruction. **Example 1: Using RST instruction**  **Example 2: Using RST instruction and DT90401** 	A	N/A
-	DT90402	**Second error alarm relay which went on (Available PLC: FP2SH/ FP10SH)**	The error alarm relay number which went on is stored. To reset the specified error alarm relay, use an RST instruction only. 		
-	DT90403	**Third error alarm relay which went on (Available PLC: FP2SH/ FP10SH)**			
-	DT90404	**Forth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)**			
-	DT90405	**Fifth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)**			
-	DT90406	**Sixth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)**			
-	DT90407	**Seventh error alarm relay which went on (Available PLC: FP2SH/ FP10SH)**			

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-
ing</th><th rowspan="2">Writ-
ing</th></tr>
<tr><th>FP3</th><th>FP2/
FP2SH
FP10SH</th></tr>
<tr><td>-</td><td>DT90408</td><td>Eighth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td><td rowspan="7">The error alarm relay number which went on is stored. To reset the specified error alarm relay, use an RST instruction only.

</td><td rowspan="7">A</td><td rowspan="7">N/A</td></tr>
<tr><td>-</td><td>DT90409</td><td>Ninth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
<tr><td>-</td><td>DT90410</td><td>Tenth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
<tr><td>-</td><td>DT90411</td><td>Eleventh error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
<tr><td>-</td><td>DT90412</td><td>Twelfth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
<tr><td>-</td><td>DT90413</td><td>Thirteenth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
<tr><td>-</td><td>DT90414</td><td>Fourteenth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
</table>

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Descriptions</th><th rowspan="2">Read-ing</th><th rowspan="2">Writ-ing</th></tr>
<tr><th>FP3</th><th>FP2/ FP2SH FP10SH</th></tr>
<tr><td>-</td><td>DT90415</td><td>Fifteenth alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td><td rowspan="5">The error alarm relay number which went on is stored. To reset the specified error alarm relay, use an RST instruction only.

</td><td rowspan="5">A</td><td rowspan="5">N/A</td></tr>
<tr><td>-</td><td>DT90416</td><td>Sixteenth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
<tr><td>-</td><td>DT90417</td><td>Seventeenth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
<tr><td>-</td><td>DT90418</td><td>Eighteenth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
<tr><td>-</td><td>DT90419</td><td>Nineteenth error alarm relay which went on (Available PLC: FP2SH/ FP10SH)</td></tr>
</table>

FP2/FP2SH/FP10SH/FP3 (A: Available, N/A: Not available)

Address		Name	Descriptions	Reading	Writing
FP3	FP2/ FP2SH FP10SH				
-	**DT90420**	**Time at which the first error alarm relay (DT90401) went on (for minute and second data) (Available PLC: FP2SH/ FP10SH)**	The time (minute and second) data at which the first error alarm relay in DT90401 went on is stored.	A	N/A
-	**DT90421**	**Time at which the first error alarm relay (DT90401) went on (for day and hour data) (Available PLC: FP2SH/ FP10SH)**	The time (day and hour) data at which the first error alarm relay in DT90401 went on is stored.		
	DT90422	**Time at which the first error alarm relay (DT90401) went on (for year and month data) (Available PLC: FP2SH/ FP10SH)**	The time (year and month) data at which the first error alarm relay in DT90401 went on is stored.		

11.2 Table of Basic Instructions

Name	Boolean	Symbol	Description	Steps *3	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Sequence basic instructions										
Start	**ST**	X,Y,R,T,C,L,P,E	Begins a logic operation with a Form A (normally open) contact.	1 (2)	○	○	○	○	○	○
Start Not	**ST/**	X,Y,R,T,C,L,P,E	Begins a logic operation with a Form B (normally closed) contact.	1 (2)	○	○	○	○	○	○
Out	**OT**	Y,R,L,E	Outputs the operated result to the specified output.	1 (2)	○	○	○	○	○	○
Not	**/**		Inverts the operated result up to this instruction.	1	○	○	○	○	○	○
AND	**AN**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact serially.	1 (2)	○	○	○	○	○	○
AND Not	**AN/**	X,Y,R,T,C,L,P,E	Connects a Form B (normally closed) contact serially.	1 (2)	○	○	○	○	○	○
OR	**OR**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact in parallel.	1 (2)	○	○	○	○	○	○
OR Not	**OR/**	X,Y,R,T,C,L,P,E	Connects a Form B (normally closed) contact in parallel.	1 (2)	○	○	○	○	○	○
Leading edge start	**ST↑**	X,Y,R,T,C,L,P,E	Begins a logic operation only for one scan when the leading edge of the trigger is detected.	2	×	○	△ *2	△ *2	○	○
Trailing edge start	**ST↓**	X,Y,R,T,C,L,P,E	Begins a logic operation only for one scan when the trailing edge of the trigger is detected.	2	×	○	△ *2	△ *2	○	○
Leading edge AND	**AN↑**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact serially only for one scan when the leading edge of the trigger is detected.	2	×	○	△ *2	△ *2	○	○
Trailing edge AND	**AN↓**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact serially only for one scan when the trailing edge of the trigger is detected.	2	×	○	△ *2	△ *2	○	○
Leading edge OR	**OR↑**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact in parallel only for one scan when the leading edge of the trigger is detected.	2	×	○	△ *2	△ *2	○	○
Trailing edge OR	**OR↓**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact in parallel only for one scan when the trailing edge of the trigger is detected.	2	×	○	△ *2	△ *2	○	○
Leading edge out	**OT↑**	P	Outputs the operated result to the specified output only for one scan when leading edge of the trigger is detected. (for pulse relay)	2	×	×	×	×	○	○
Trailing edge out	**OT↓**	P	Outputs the operated result to the specified output only for one scan when trailing edge of the trigger is detected. (for pulse relay)	2	×	×	×	×	○	○
Alterna-tive out	**ALT**	Y,R,L,E	Inverts the output condition (on/off) each time the leading edge of the trigger is detected.	3	×	○	○	○	○	○
AND stack	**ANS**		Connects the multiple instruction blocks serially.	1	○	○	○	○	○	○
OR stack	**ORS**		Connects the multiple instruction blocks in parallel.	1	○	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

*1) The type of the devices that can be specified depends on the models.

*2) This instruction is available for FP-X Ver. 2.0 or later, and FPΣ Ver. 3.10 or later.

*3) In the FP2/FP2SH/10SH, when using X1280, Y1280, R1120 (special internal relay included), L1280, T256, C256 or anything beyond for the ST, ST/, OT, AN, AN/, OR and OR/ instructions, the number of steps is shown in parentheses. Also, in the FP2/FP2SH/FP10SH, when a relay number has an index modifier, the number of steps is shown in parentheses. For the FPΣ and FP-X, the number of steps varies according to the relay number to be used.

Name	Boolean	Symbol	Description	Steps *5 *6	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Push stack	**PSHS**		Stores the operated result up to this instruction. *2	1	○	○	○	○	○	○
Read stack	**RDS**		Reads the operated result stored by the PSHS instruction. *2	1	○	○	○	○	○	○
Pop stack	**POPS**		Reads and clears the operated result stored by the PSHS instruction	1	○	○	○	○	○	○
Leading edge differential	**DF**	(DF)	Turns on the contact for only one scan when the leading edge of the trigger is detected.	1	○	○	○	○	○	○
Trailing edge differential	**DF/**	(DF/)	Turns on the contact for only one scan when the trailing edge of the trigger is detected.	1	○	○	○	○	○	○
Leading edge differential (initial execution type)	**DFI**	(DFI)	Turns on the contact for only one scan when the leading edge of the trigger is detected. The leading edge detection is possible on the first scan.	1	×	○	○	○	○	○
Set	**SET**	Y, R, L, E ⟨S⟩	Output is set to and held at on.	3	○	○	○	○	○	○
Reset	**RST**	Y, R, L, E ⟨R⟩	Output is set to and held at off.	3	○	○	○	○	○	○
Keep	**KP**	Reset	Outputs at set trigger and holds until reset trigger turns on.	1 (2)	○	○	○	○	○	○
No operation	**NOP**	●	No operation.	1	○	○	○	○	○	○
Basic function instructions										
On-delay timer	**TML**	TMa, n	After set value "n" x 0.001 seconds, timer contact "a" is set to on.	3 (4)	○	○	○	○	○	○ *3
	TMR		After set value "n" x 0.01 seconds, timer contact "a" is set to on.	3 (4)	○	○	○	○	○	○ *3
	TMX		After set value "n" x 0.1 seconds, timer contact "a" is set to on.	3 (4)	○	○	○	○	○	○ *3
	TMY		After set value "n" x 1 second, timer contact "a" is set to on.	4 (5)	○	○	○	○	○	○ *3
Auxiliary timer (16-bit)	**F137 (STMR)**	F137 STMR S, D Y,R,L,E	After set value "S" x 0.01 seconds, the specified output and R900D are set to on.	5	○	○	○	○	○	○
Auxiliary timer (32-bit)	**F183 (DSTM)**	F183 DSTM S, D Y,R,L,E	After set value "S" x 0.01 seconds, the specified output and R900D are set to on.	7	○	○	○	○	○	○
Time constant processing	**F182**	F182 FILTR S1, S2, S3, D	Executes the filter processing for the specified input.	9	×	○	○	○	×	×
Counter	**CT**	Count CT Reset n	Decrements from the preset value "n"	3 (4)	○	○	○	○	○	○ *3

○ : Available, × : Not available, △ : Not available partially

*1) The type of the devices that can be specified depends on the models.

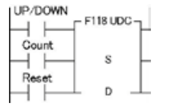
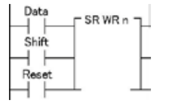
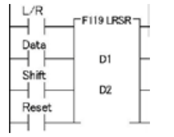
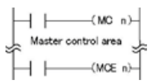
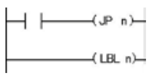
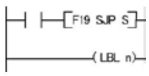
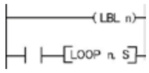
*2) The allowable number of using the PSHS and RDS instruction depends on the models.

*3) For FP2SH, FP10SH and FP-X Ver2.0 or later, any device can be set for the setting value of counter or timer instruction.

*4) This instruction is available for FP-X Ver. 2.0 or later.

*5) In the FP2/FP2SH/FP10SH, when using Y1280, R1120 (special internal relay included), L1280 or anything beyond for the KP instruction, the number of steps is shown in parentheses. Also, in the FP2/FP2SH/FP10SH, when a relay number has an index modifier, the number of steps is shown in parentheses.

*6) In the FP2/FP2SH/FP10SH, when timer 256 or higher, or counter 255 or lower, is used, the number of steps is the number in parentheses. Also, in the FP2/FP2SH/FP10SH, when a timer number or counter number has an index modifier, the number of steps is the number in parentheses. For the FPΣ and FP-X, the number of steps varies according to the specified timer number or counter number.

Name	Boolean	Symbol	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
UP/DOWN counter	**F118 (UDC)**		Increments or decrements from the preset value “S” based on up/down input.	5	○	○	○	○	○	○
Shift register	**SR**		Shifts one bit of 16-bit [word internal relay (WR)] data to the left.	1 (2) *1	○	○	○	○	○	○
Left/right shift register	**F119 (LRSR)**		Shifts one bit of 16-bit data range specified by “D1” and “D2” to the left or to the right.	5	○	○	○	○	○	○
Control instructions										
Master control relay	**MC**		Starts the master control program.	2	○	○	○	○	○	○
Master control relay end	**MCE**		Ends the master control program.	2	○	○	○	○	○	○
Jump **Label**	**JP** **LBL**		The program jumps to the label instruction and continues from there.	2 (3) *2 1	○	○	○	○	○	○
Auxiliary jump **Label**	**F19 (SJP)** **LBL**		The program jumps to the label instruction specified by “S” and continues from there.	3 1	×	×	×	×	○	○
Loop **Label**	**LOOP** **LBL**		The program jumps to the label instruction and continues from there (the number of jumps is set in “S”).	4 (5) *3 1	○	○	○	○	○	○
Break	**BRK**		Stops program execution when the predetermined trigger turns on in the TEST/RUN mode only.	1	×	×	×	×	○	○

○ : Available, × : Not available, △ : Not available partially

*1) In the FP2/FP2SH/FP10SH, when internal relay WR240 or higher is used, the number of steps is the number in parentheses. Also, in the FP2/FP2SH/FP10SH, when the specified internal relay number (word address) has an index modifier, the number of steps is the number in parentheses.

*2) In the FP2/FP2SH/FP10SH, when the number “n” in a jump instruction has an index modifier, the number of steps isthenumber in parentheses.

*3) In the FP2/FP2SH/FP10SH, when the number “n” in a loop instruction has an index modifier, the number of steps is the number in parentheses.

Name	Boolean	Symbol	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
End	**ED**	(ED)	The operation of program is ended. Indicates the end of a main program.	1	○	○	○	○	○	○
Conditional end	**CNDE**	(CNDE)	The operation of program is ended when the trigger turns on.	1	○	○	○	○	○	○
Eject	**EJECT**	(EJECT)	Adds page break for use when printing.	1	×	○	○	○	○	○
Step ladder instructions										
Start step	**SSTP**	(SSTP n)	The start of program “n” for process control	3	○	○	○	○	○	○
Next step	**NSTL**	(NSTL n)	Starts the specified process “n” and clears the process currently started. (Scan execution type)	3	○	○	○	○	○	○
	NSTP	(NSTP n)	Starts the specified process “n” and clears the process currently started. (Pulse execution type)	3	○	○	○	○	○	○
Clear step	**CSTP**	(CSTP n)	Resets the specified process “n”.	3	○	○	○	○	○	○
Clear multi-ple steps	**SCLR**	[SCLR n1, n2]	Resets multiple processes specified by “n1” and “n2”.	5	△ *1	○	○	○	○	○
Step end	**STPE**	(STPE)	End of step ladder area	1	○	○	○	○	○	○
Subroutine instructions										
Subroutine call	**CALL**	(CALL n)	When the trigger is on: Executes the subroutine. When the trigger is off: Not execute the subroutine. The output in the subroutine is maintained.	2 (3) *2	○	○	○	○	○	○
Output off type subroutine call	**FCAL**	(FCAL n)	When the trigger is on: Executes the subroutine. When the trigger is off: Not execute the subroutine. But, the output in the subroutine is cleared.	4 (5) *2	×	×	×	×	×	○
Subroutine entry	**SUB**	(SUB n)	Indicates the start of the subroutine program “n”.	1	○	○	○	○	○	○
Subroutine return	**RET**	(RET)	Ends the subroutine program.	1	○	○	○	○	○	○
Interrupt instructions										
Interrupt	**INT**	(INT n)	Indicates the start of the interrupt program “n”.	1	○	○	○	○	○	○
Interrupt return	**IRET**	(IRET)	Ends the interrupt program.	1	○	○	○	○	○	○
Interrupt control	**ICTL**	(DF) [ICTL S1, S2]	Select interrupt enable/disable or clear in “S1” and “S2” and execute.	5	○	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

*1) Available for FP-e only.

*2) In the FP2/FP2SH/FP10SH, when the number “n” of a subroutine program has an index modifier, the number of steps is the number in parentheses.

Name	Boolean	Symbol	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Special setting instructions										
Communica-tion condi-tions setting	**SYS1**	├ ├(DF)┤[SYS1, M]	Change the communication conditions for the COM port or tool port based on the contents specified by the character constant.	13	×	○	○ *1	○ *1	×	×
Password setting			Change the password specified by the PLC based on the contents specified by the character constant.		×	○	○ *2	○	×	×
Interrupt setting			Set the interrupt input based on the contents specified by the character constant.		×	○	○	○	×	×
PLC link time setting			Set the system setting time when a PLC link is used, based on the contents specified by the character constant.		×	○	○	○	×	×
MEWTOCOL-COM response control			Change the communication conditions of the COM. port or tool port for MEWTOCOL-COM based on the contents specified by the character constant.		×	○	○	○	×	×
High-speed counter operation mode changing			Change the operation mode of the high-speed counter, based on the contents specified by the character constant.		×	○	○ *3	○ *3	×	×
System registers "No. 40 to No. 47" changing	**SYS2**	├ ├[SYS2, S, D1, D2]┤	Change the setting value of the system register for the PLC link function.	7	×	○	○	○	×	×

○ : Available, × : Not available, △ : Not available partially

*1) With FP-X Ver2.0 or later, and FPΣ Ver 3.10 or later, the baud rate can be selected from 300, 600 or 1200 bps.

*2) With FPΣ 32k type, the 8-digit password can be selected.

*3) With FPΣ 32k type and FP-X Ver1.10 or later, it can be used.

Name	Boolean	Symbol	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Data compare instructions										
16-bit data compare (Start)	**ST=**	= S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1=S2”.	5	○	○	○	○	○	○
	ST<>	< > S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1<S2” or “S1>S2”.	5	○	○	○	○	○	○
	ST>	> S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1>S2”.	5	○	○	○	○	○	○
	ST>=	>= S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1>S2” or “S1=S2”.	5	○	○	○	○	○	○
	ST<	< S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1<S2”.	5	○	○	○	○	○	○
	ST<=	<= S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1<S2” or “S1=S2”.	5	○	○	○	○	○	○
16-bit data compare (AND)	**AN=**	= S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1=S2”.	5	○	○	○	○	○	○
	AN<>	< > S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1<S2” or “S1>S2”.	5	○	○	○	○	○	○
	AN>	> S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1>S2”.	5	○	○	○	○	○	○
	AN>=	>= S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1>S2” or “S1=S2”.	5	○	○	○	○	○	○
	AN<	< S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1<S2”.	5	○	○	○	○	○	○
	AN<=	<= S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1<S2” or “S1=S2”.	5	○	○	○	○	○	○
16-bit data compare (OR)	**OR=**	= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1=S2”.	5	○	○	○	○	○	○
	OR<>	< > S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1<S2” or “S1>S2”.	5	○	○	○	○	○	○
	OR>	> S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1>S2”.	5	○	○	○	○	○	○
	OR>=	>= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1>S2” or “S1=S2”.	5	○	○	○	○	○	○
	OR<	< S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1<S2”.	5	○	○	○	○	○	○
	OR<=	<= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1<S2” or “S1=S2”.	5	○	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

Name	Boolean	Symbol	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
32-bit data compare (Start)	**STD=**	D= S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)=(S2+1, S2)”.	9	○	○	○	○	○	○
	STD<>	D<> S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)>(S2+1, S2)”.	9	○	○	○	○	○	○
	STD>	D> S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)”.	9	○	○	○	○	○	○
	STD>=	D>= S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	○	○	○	○	○	○
	STD<	D< S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)”.	9	○	○	○	○	○	○
	STD<=	D<= S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	○	○	○	○	○	○
32-bit data compare (AND)	**AND=**	D= S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)=(S2+1, S2)”.	9	○	○	○	○	○	○
	AND<>	D<> S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)>(S2+1, S2)”.	9	○	○	○	○	○	○
	AND>	D> S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)”.	9	○	○	○	○	○	○
	AND>=	D>= S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	○	○	○	○	○	○
	AND<	D< S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)”.	9	○	○	○	○	○	○
	AND<=	D<= S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	○	○	○	○	○	○
32-bit data compare (OR)	**ORD=**	D= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)=(S2+1, S2)”.	9	○	○	○	○	○	○
	ORD<>	D<> S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)>(S2+1, S2)”.	9	○	○	○	○	○	○
	ORD>	D> S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)”.	9	○	○	○	○	○	○
	ORD>=	D>= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	○	○	○	○	○	○
	ORD<	D< S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)”.	9	○	○	○	○	○	○
	ORD<=	D<= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	○	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

Name	Boolean	Symbol	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Floating point type real number data compare (Start)	**STF=**	F= S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)=(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	STF<>	F<> S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)>(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	STF>	F> S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	STF>=	F>= S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	STF<	F< S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	STF<=	F<= S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
Floating point type real number data compare (AND)	**ANF=**	F= S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)=(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ANF<>	F<> S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)>(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ANF>	F> S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ANF>=	F>= S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ANF<	F< S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ANF<=	F<= S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
Floating point type real number data compare (OR)	**ORF=**	F= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)=(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ORF<>	F<> S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)>(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ORF>	F> S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ORF>=	F>= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ORF<	F< S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×
	ORF<=	F<= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2)” or “(S1+1, S1)=(S2+1, S2)”.	9	×	○	△ *1	△ *1	×	×

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is available for FP-X V1.10 or later and FPΣ 32k type

11.3 Table of High-level Instructions

The high-level instructions are expressed by the prefixes “F” or “P” with numbers. For most of the high-level instructions, “F” and “P” types are available. The differences between the two types are explained as follows:
- Instructions with the prefix “F” are executed in every scan while its trigger is in the on.
- Instructions with the prefix “P” are executed only when the leading edge of its trigger is detected.
For the FP0/FP0R/FPΣ/FP-X, the P type high-level instructions are not available.

Number	Name	Boolean	Operand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Data transfer instructions											
F0 P0	**16-bit data move**	**MV PMV**	S, D	(S)→(D)	5	○	○	○	○	○	○
F1 P1	**32-bit data move**	**DMV PDMV**	S, D	(S+1, S)→(D+1, D)	7	○	○	○	○	○	○
F2 P2	**16-bit data invert and move**	**MV PMV/**	S, D	(S)→(D)	5	○	○	○	○	○	○
F3 P3	**32-bit data invert and move**	**DMV/ PDMV/**	S, D	$\overline{(S+1, S)}$→(D+1, D)	7	○	○	○	○	○	○
F4 P4	**Reading of head word No. of the specified slot**	**GETS PGETS**	S, D	The head word No. of the specified slot is read.	5	×	×	×	×	△ *1	△ *1
F5 P5	**Bit data move**	**BTM PBTM**	S, n, D	The specified one bit in “S” is transferred to the specified one bit in “D”. The bit is specified by “n”.	7	○	○	○	○	○	○
F6 P6	**Hexadecimal digit (4-bit) data move**	**DGT PDGT**	S, n, d	The specified one digit in “S” is transferred to the specified one digit in “D”. The digit is specified by “n”.	7	○	○	○	○	○	○
F7 P7	**Two 16-bit data move**	**MV2 PMV2**	S1, S2, D	(S1)→(D), (S2)→(D+1)	7	×	○	○	○	○	○
F8 P8	**Two 32-bit data move**	**DMV2 PDMV2**	S1, S2, D	(S1+1, S1)→(D+1, D), (S2+1, S2)→(D+3, D+2)	11	×	○	○	○	○	○
F10 P10	**Block move**	**BKMV PBKMV**	S1, S2, D	The data between “S1” and “S2” is transferred to the area starting at “D”.	7	○	○	○	○	○	○
F11 P11	**Block copy**	**COPY PCOPY**	S, D1, D2	The data of “S” is transferred to the all area between “D1” and “D2”.	7	○	○	○	○	○	○
F12	**Data read from EEP-ROM**	**ICRD**	S1, S2, D	The data stored in the expansion memory of the EEP-ROM specified by “S1” and “S2” are transferred to the area starting at “D”.	11	○ *2	×	×	×	×	×
P13	**Data write to EEP-ROM**	**PICWT**	S1, S2, D	The data specified by “S1” and “S2” are transferred to the EEP-ROM starting at “D”.	11	○ *2	×	×	×	×	×
F12	**Data read from F-ROM**	**ICRD**	S1, S2, D	The data stored in the expansion memory of the F-ROM specified by “S1” and “S2” are transferred to the area starting at “D”.	11	×	○	○	○	×	×
P13	**Data write to F-ROM**	**PICWT**	S1, S2, D	The data specified by “S1” and “S2” are transferred to the F-ROM starting at “D”.	11	×	○	○	○	×	×
F12 P12	**Data read from IC card**	**ICRD PICRD**	S1, S2, D	The data stored in the expansion memory of the IC card specified by “S1” and “S2” are transferred to the area starting at “D”.	11	×	×	×	×	×	○
F13 P13	**Data write to IC card**	**ICWT PICWT**	S1, S2, D	The data specified by “S1” and “S2” are transferred to the IC card expansion memory area starting at “D”.	11	×	×	×	×	×	○
F14 P14	**Program read from IC memory card**	**PGRD PPGRD**	S	The program specified using “S” is transferred into the CPU from IC memory card and executes it.	3	×	×	×	×	×	○

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is available for FP2/FP2SH Ver. 1.5 or later.FP10SH cannot be used

*2) This instruction is available for FP0 Ver. 2.0 or later and FP-e.

Num-ber	Name	Boo-lean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F15 P15	**16-bit data exchange**	**XCH PXCH**	D1, D2	(D1)→(D2), (D2)→(D1)	5	○	○	○	○	○	○
F16 P16	**32-bit data exchange**	**DXCH PDXCH**	D1, D2	(D1+1, D1)→(D2+1, D2) (D2+1, D2)→(D1+1, D1)	5	○	○	○	○	○	○
F17 P17	**Higher/lower byte in 16-bit data exchange**	**SWAP PSWAP**	D	The higher byte and lower byte of "D" are exchanged.	3	○	○	○	○	○	○
F18 P18	**16-bit data block exchange**	**BXCH PBXCH**	D1, D2, D3	Exchange the data between "D1" and "D2" with the data specified by "D3".	7	×	○	○	○	○	○
Control instruction											
F19	**Auxiliary jump**	**SJP**	S	The program jumps to the label instruction specified by "S" and continues from there.	3	×	×	×	×	○	○
Binary arithmetic instructions											
F20 P20	**16-bit data addition**	**+ P+**	S, D	(D)+(S)→(D)	5	○	○	○	○	○	○
F21 P21	**32-bit data addition**	**D+ PD+**	S, D	(D+1, D)+(S+1, S)→(D+1, D)	7	○	○	○	○	○	○
F22 P22	**16-bit data addition**	**+ P+**	S1, S2, D	(S1)+(S2)→(D)	7	○	○	○	○	○	○
F23 P23	**32-bit data addition**	**D+ PD+**	S1, S2, D	(S1+1, S1)+(S2+1, S2)→(D+1, D)	11	○	○	○	○	○	○
F25 P25	**16-bit data subtraction**	**- P-**	S, D	(D)-(S)→(D)	5	○	○	○	○	○	○
F26 P26	**32-bit data subtraction**	**D- PD-**	S, D	(D+1, D)-(S+1, S)→(D+1, D)	7	○	○	○	○	○	○
F27 P27	**16-bit data subtraction**	**- P-**	S1, S2, D	(S1)-(S2)→(D)	7	○	○	○	○	○	○
F28 P28	**32-bit data subtraction**	**D- PD-**	S1, S2, D	(S1+1, S1)-(S2+1, S2)→(D+1, D)	11	○	○	○	○	○	○
F30 P30	**16-bit data multiplication**	*** P***	S1, S2, D	(S1)X(S2)→(D+1, D)	7	○	○	○	○	○	○
F31 P31	**32-bit data multiplication**	**D* PD***	S1, S2, D	(S1+1, S1)X(S2+1, S2)→(D+3, D+2, D+1, D)	11	○	○	○	○	○	○
F32 P32	**16-bit data division**	**% P%**	S1, S2, D	(S1)÷(S2)→quotient (D) remainder (DT9015)	7	○	○	○	○	○	○
F33 P33	**32-bit data division**	**D% PD%**	S1, S2, D	(S1+1, S1)÷(S2+1, S2)→quotient (D+1, D) remainder (DT9016, DT9015)	11	○	○	○	○	○	○
F34 P34	**16-bit data multiplication (result in 16 bits)**	***W P*W**	S1, S2, D	(S1)X(S2)→(D)	7	×	○	○	○	○	○
F35 P35	**16-bit data increment**	**+1 P+1**	D	(D)+1→(D)	3	○	○	○	○	○	○
F36 P36	**32-bit data increment**	**D+1 PD+1**	D	(D+1, D)+1→(D+1, D)	3	○	○	○	○	○	○
F37 P37	**16-bit data decrement**	**-1 P-1**	D	(D)-1→(D)	3	○	○	○	○	○	○
F38 P38	**32-bit data decrement**	**D-1 PD-1**	D	(D+1, D)-1→(D+1, D)	3	○	○	○	○	○	○
F39 P39	**32-bit data multiplication (result in 32 bits)**	**D*D PD*D**	S1, S2, D	(S1+1, S1)x(S2+1, S2)→(D+1, D)	11	×	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

Num-ber	Name	Boo-lean	Operand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
BCD arithmetic instructions											
F40 P40	**4-digit BCD data addition**	**B+ PB+**	S, D	(D)+(S)→(D)	5	○	○	○	○	○	○
F41 P41	**8-digit BCD data addition**	**DB+ PDB+**	S, D	(D+1, D)+(S+1, S)→(D+1, D)	7	○	○	○	○	○	○
F42 P42	**4-digit BCD data addition**	**B+ PB+**	S1, S2, D	(S1)+(S2)→(D)	7	○	○	○	○	○	○
F43 P43	**8-digit BCD data addition**	**DB+ PDB+**	S1, S2, D	(S1+1, S1)+(S2+1, S2)→(D+1, D)	11	○	○	○	○	○	○
F45 P45	**4-digit BCD data subtraction**	**B- PB-**	S, D	(D)-(S)→(D)	5	○	○	○	○	○	○
F46 P46	**8-digit BCD data subtraction**	**DB- PDB-**	S, D	(D+1, D)-(S+1, S)→(D+1, D)	7	○	○	○	○	○	○
F47 P47	**4-digit BCD data subtraction**	**B- PB-**	S1, S2, D	(S1)-(S2)→(D)	7	○	○	○	○	○	○
F48 P48	**8-digit BCD data subtraction**	**DB- PDB-**	S1, S2, D	(S1+1, S1)-(S2+1, S2)→(D+1, D)	11	○	○	○	○	○	○
F50 P50	**4-digit BCD data multiplication**	**B* PB***	S1, S2, D	(S1)X(S2)→(D+1, D)	7	○	○	○	○	○	○
F51 P51	**8-digit BCD data multiplication**	**DB* PDB***	S1, S2, D	(S1+1, S1)X(S2+1, S2)→(D+3, D+2, D+1, D)	11	○	○	○	○	○	○
F52 P52	**4-digit BCD data division**	**B% PB%**	S1, S2, D	(S1)÷(S2)→quotient (D) remainder (DT9015)	7	○	○	○	○	○	○
F53 P53	**8-digit BCD data division**	**DB% PDB%**	S1, S2, D	(S1+1, S1)÷(S2+1, S2)→quotient (D+1, D) remainder (DT9016, DT9015)	11	○	○	○	○	○	○
F55 P55	**4-digit BCD data increment**	**B+1 PB+1**	D	(D)+1→(D)	3	○	○	○	○	○	○
F56 P56	**8-digit BCD data increment**	**DB+1 PDB+1**	D	(D+1, D)+1→(D+1, D)	3	○	○	○	○	○	○
F57 P57	**4-digit BCD data decrement**	**B-1 PB-1**	D	(D)-1→(D)	3	○	○	○	○	○	○
F58 P58	**8-digit BCD data decrement**	**DB-1 PDB-1**	D	(D+1, D)-1→(D+1, D)	3	○	○	○	○	○	○
Data compare instructions											
F60 P60	**16-bit data compare**	**CMP PCMP**	S1, S2	(S1)>(S2)→R900A: on (S1)=(S2)→R900B: on (S1)<(S2)→R900C: on	5	○	○	○	○	○	○
F61 P61	**32-bit data compare**	**DCMP PDCMP**	S1, S2	(S1+1, S1)>(S2+1, S2)→R900A: on (S1+1, S1)=(S2+1, S2)→R900B: on (S1+1, S1)<(S2+1, S2)→R900C: on	9	○	○	○	○	○	○
F62 P62	**16-bit data band compare**	**WIN PWIN**	S1, S2, S3	(S1)>(S3)→R900A: on (S2)< or=(S1)< or=(S3)→R900B: on (S1)<(S2)→R900C: on	7	○	○	○	○	○	○

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Num-ber	Name	Boo-lean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F63 **P63**	**32-bit data band compare**	**DWIN** **PDWIN**	S1, S2, S3	(S1+1, S1)>(S3+1, S3)→R900A: on (S2+1, S2)< or=(S1+1, S1)< or=(S3+1, S3)→R900B: on (S1+1, S1)<(S2+1, S2)→R900C: on	13	○	○	○	○	○	○
F64 **P64**	**Block data compare**	**BCMP** **PBCMP**	S1, S2, S3	Compares the two blocks beginning with “S2” and “S3” to see if they are equal.	7	○	○	○	○	○	○
Logic operation instructions											
F65 **P65**	**16-bit data AND**	**WAN** **PWAN**	S1, S2, D	(S1) AND (S2)→(D)	7	○	○	○	○	○	○
F66 **P66**	**16-bit data OR**	**WOR** **PWOR**	S1, S2, D	(S1) OR (S2)→(D)	7	○	○	○	○	○	○
F67 **P67**	**16-bit data exclusive OR**	**XOR** **PXOR**	S1, S2, D	{(S1) AND $\overline{(S2)}$} OR {$\overline{(S1)}$ AND (S2)}→(D)	7	○	○	○	○	○	○
F68 **P68**	**16-bit data exclusive NOR**	**XNR** **PXNR**	S1, S2, D	{(S1) AND (S2)} OR {$\overline{(S1)}$ AND $\overline{(S2)}$}→(D)	7	○	○	○	○	○	○
F69 **P69**	**16-bit data unite**	**WUNI** **PWUNI**	S1, S2, S3, D	([S1] AND [S3]) OR ([S2] AND $\overline{[S3]}$)→(D) When (S3) is H0, (S2)→(D) When (S3) is HFFFF, (S1) →(D)	9	×	○	○	○	○	○
Data conversion instructions											
F70 **P70**	**Block check code calculation**	**BCC** **PBCC**	S1, S2, S3, D	Creates the code for checking the data specified by “S2” and “S3” and stores it in “D”. The calculation method is specified by “S1”.	9	○	○	○	○	○	○
F71 **P71**	**Hexadecimal data → ASCII code**	**HEXA** **PHEXA**	S1, S2, D	Converts the hexadecimal data specified by “S1” and “S2” to ASCII code and stores it in “D”. Example: HABCD→ H 42 41 44 43 B A D C	7	○	○	○	○	○	○
F72 **P72**	**ASCII code → Hexadeci-mal data**	**AHEX** **PAHEX**	S1, S2, D	Converts the ASCII code specified by “S1” and “S2” to hexadecimal data and stores it in “D”. Example: H 44 43 42 41 → HCDAB D C B A	7	○	○	○	○	○	○
F73 **P73**	**4-digit BCD data → ASCII code**	**BCDA** **PBCDA**	S1, S2, D	Converts the four digits of BCD data specified by “S1” and “S2” to ASCII code and stores it in “D”. Example: H1234→ H 32 31 34 33 2 1 4 3	7	○	○	○	○	○	○
F74 **P74**	**ASCII code → 4-digit BCD data**	**ABCD** **PABCD**	S1, S2, D	Converts the ASCII code specified by “S1” and “S2” to four digits of BCD data and stores it in “D”. Example: H 34 33 32 31 → H3412 4 3 2 1	9	○	○	○	○	○	○
F75 **P75**	**16-bit binary data → ASCII code**	**BINA** **PBINA**	S1, S2, D	Converts the 16 bits of binary data specified by “S1” to ASCII code and stores it in “D” (area of “S2” bytes). Example: K-100→ H 30 30 31 2D 20 20 0 0 1 -	7	○	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

Num-ber	Name	Boolean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F76 **P76**	**ASCII code → 16-bit binary data**	**ABIN** **PABIN**	S1, S2, D	Converts the ASCII code specified by “S1” and “S2” to 16 bits of binary data and stores it in “D”. Example: H 30 30 31 2D 20 20 → K-100 0 0 1 -	7	○	○	○	○	○	○
F77 **P77**	**32-bit binary data → ASCII code**	**DBIA** **PDBIA**	S1, S2, D	Converts the 32 bits of binary data (S1+1, S1) to ASCII code and stores it in D (area of “S2” bytes).	11	○	○	○	○	○	○
F78 **P78**	**ASCII code → 32-bit binary data**	**DABI** **PDABI**	S1, S2, D	Converts the ASCII code specified by “S1” and “S2” to 32 bits of binary data and stores it in (D+1, D).	11	○	○	○	○	○	○
F80 **P80**	**16-bit binary data → 4-digit BCD data**	**BCD** **PBCD**	S, D	Converts the 16 bits of binary data specified by “S” to four digits of BCD data and stores it in “D”. Example: K100 → H100	5	○	○	○	○	○	○
F81 **P81**	**4-digit BCD data → 16-bit binary data**	**BIN** **PBIN**	S, D	Converts the four digits of BCD data specified by “S” to 16 bits of binary data and stores it in “D”. Example: H100 → K100	5	○	○	○	○	○	○
F82 **P82**	**32-bit binary data → 8-digit BCD data**	**DBCD** **PDBCD**	S, D	Converts the 32 bits of binary data specified by (S+1, S) to eight digits of BCD data and stores it in (D+1, D).	7	○	○	○	○	○	○
F83 **P83**	**8-digit BCD data → 32-bit binary data**	**DBIN** **PDBIN**	S, D	Converts the eight digits of BCD data specified by (S+1, S) to 32 bits of binary data and stores it in (D+1, D).	7	○	○	○	○	○	○
F84 **P84**	**16-bit data invert (com-plement of 1)**	**INV** **PINV**	D	Inverts each bit of data of “D”.	3	○	○	○	○	○	○
F85 **P85**	**16-bit data complement of 2**	**NEG** **PNEG**	D	Inverts each bit of data of “D” and adds 1 (inverts the sign).	3	○	○	○	○	○	○
F86 **P86**	**32-bit data complement of 2**	**DNEG** **PDNEG**	D	Inverts each bit of data of (D+1, D) and adds 1 (inverts the sign).	3	○	○	○	○	○	○
F87 **P87**	**16-bit data absolute**	**ABS** **PABS**	D	Gives the absolute value of the data of “D”.	3	○	○	○	○	○	○
F88 **P88**	**32-bit data absolute**	**DABS** **PDABS**	D	Gives the absolute value of the data of (D+1, D).	3	○	○	○	○	○	○
F89 **P89**	**16-bit data sign extension**	**EXT** **PEXT**	D	Extends the 16 bits of data in “D” to 32 bits in (D+1, D).	3	○	○	○	○	○	○
F90 **P90**	**Decode**	**DECO** **PDECO**	S, n, D	Decodes part of the data of “S” and stores it in “D”. The part is specified by “n”.	7	○	○	○	○	○	○
F91 **P91**	**7-segment decode**	**SEGT** **PSEGT**	S, D	Converts the data of “S” for use in a 7-segment display and stores it in (D+1, D).	5	○	○	○	○	○	○
F92 **P92**	**Encode**	**ENCO** **PENCO**	S, n, D	Encodes part of the data of “S” and stores it in “D”. The part is specified by “n”.	7	○	○	○	○	○	○
F93 **P93**	**16-bit data combine**	**UNIT** **PUNIT**	S, n, D	The least significant digit of each of the “n” words of data beginning at “S” are stored (united) in order in “D”.	7	○	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

Num-ber	Name	Boo-lean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F94 **P94**	**16-bit data distribute**	**DIST** **PDIST**	S, n, D	Each of the digits of the data of “S” are stored in (distributed to) the least significant digits of the areas beginning at “D”.	7	○	○	○	○	○	○
F95 **P95**	**Character→ ASCII code**	**ASC** **PASC**	S, D	Twelve characters of the character constants of “S” are converted to ASCII code and stored in “D” to “D+5”.	15	○	○	○	○	○	○
F96 **P96**	**16-bit table data search**	**SRC** **PSRC**	S1, S2, S3	The data of “S1” is searched for in the areas in the range “S2” to “S3” and the result is stored in DT9037 and DT9038	7	○	○	○	○	○	○
F97 **P97**	**32-bit table data search**	**DSRC** **PDSRC**	S1, S2, S3	The data of (S1+1, S1) is searched for in the 32-bit data designated by “S3”, beginning from “S2”, and the result if stored in DT90037 and DT90038.	11	×	○	○	○	○	○
Data shift instructions											
F98 **P98**	**Data table shift-out and compress**	**CMPR** **PCMPR**	D1, D2, D3	Transfer “D2” to “D3”. Any parts of the data between “D1” and “D2” that are 0 are compressed, and shifted in order toward “D2”.	7	×	○	○	○	○	○
F99 **P99**	**Data table shift-in and compress**	**CMPW** **PCMP W**	S, D1, D2	Transfer “S” to “D1”. Any parts of the data between “D1” and “D2” that are 0 are compressed, and shifted in order toward “D2”.	7	×	○	○	○	○	○
F100 **P100**	**Right shift of multiple bits (n bits) in a 16-bit data**	**SHR** **PSHR**	D, n	Shifts the “n” bits of “D” to the right.	5	○	○	○	○	○	○
F101 **P101**	**Left shift of multiple bits (n bits) in a 16-bit data**	**SHL** **PSHL**	D, n	Shifts the “n” bits of “D” to the left.	5	○	○	○	○	○	○
F102 **P102**	**Right shift of n bits in a 32-bit data**	**DSHR** **PDSHR**	D, n	Shifts the “n” bits of the 32-bit data area specified by (D+1, D) to the right.	5	×	○	○	○	○	○
F103 **P103**	**Left shift of n bits in a 32-bit data**	**DSHL** **PDSHL**	D, n	Shifts the “n” bits of the 32-bit data area specified by (D+1, D) to the left.	5	×	○	○	○	○	○
F105 **P105**	**Right shift of one hexadecimal digit (4-bit)**	**BSR** **PBSR**	D	Shifts the one digit of data of “D” to the right.	3	○	○	○	○	○	○
F106 **P106**	**Left shift of one hexadecimal digit (4-bit)**	**BSL** **PBSL**	D	Shifts the one digit of data of “D” to the left.	3	○	○	○	○	○	○
F108 **P108**	**Right shift of multiple bits (n bits)**	**BITR** **PBITR**	D1, D2, n	Shifts the “n” bits of data range by “D1” and “D2” to the right.	7	×	○	○	○	○	○
F109 **P109**	**Left shift of multiple bits (n bits)**	**BITL** **PBITL**	D1, D2, n	Shifts the “n” bits of data range by “D1” and “D2” to the left.	7	×	○	○	○	○	○
F110 **P110**	**Right shift of one word (16-bit)**	**WSHR** **PWSHR**	D1, D2	Shifts the one word of the areas by “D1” and “D2” to the right.	5	○	○	○	○	○	○
F111 **P111**	**Left shift of one word (16-bit)**	**WSHL** **PWSHL**	D1, D2	Shifts the one word of the areas by “D1” and “D2” to the left.	5	○	○	○	○	○	○
F112 **P112**	**Right shift of one hexadecimal digit (4-bit)**	**WBSR** **PWBSR**	D1, D2	Shifts the one digit of the areas by “D1” and “D2” to the right.	5	○	○	○	○	○	○
F113 **P113**	**Left shift of one hexadecimal digit (4-bit)**	**WBSL** **PWBSL**	D1, D2	Shifts the one digit of the areas by “D1” and “D2” to the left.	5	○	○	○	○	○	○

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Num-ber	Name	Boolean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
FIFO instructions											
F115 **P115**	**FIFO buffer define**	**FIFT** **PFIFT**	n, D	The “n” words beginning from “D” are defined in the buffer.	5	×	○	○	○	○	○
F116 **P116**	**Data read from FIFO buffer**	**FIFR** **PFIFR**	S, D	The oldest data beginning from “S” that was written to the buffer is read and stored in “D”.	5	×	○	○	○	○	○
F117 **P117**	**Data write into FIFO buffer**	**FIFW** **PFIFW**	S, D	The data of “S” is written to the buffer starting from “D”.	5	×	○	○	○	○	○
Basic function instructions											
F118	**UP/DOWN counter**	**UDC**	S, D	Counts up or down from the value preset in “S” and stores the elapsed value in “D”.	5	○	○	○	○	○	○
F119	**Left/right shift register**	**LRSR**	D1, D2	Shifts one bit to the left or right with the area between “D1” and “D2” as the register.	5	○	○	○	○	○	○
Data rotate instructions											
F120 **P120**	**16-bit data right rotate**	**ROR** **PROR**	D, n	Rotates the “n” bits in data of “D” to the right.	5	○	○	○	○	○	○
F121 **P121**	**16-bit data left rotate**	**ROL** **PROL**	D, n	Rotates the “n” bits in data of “D” to the left.	5	○	○	○	○	○	○
F122 **P122**	**16-bit data right rotate with carry flag (R9009) data**	**RCR** **PRCR**	D, n	Rotates the “n” bits in 17-bit area consisting of “D” plus the carry flag (R9009) data to the right.	5	○	○	○	○	○	○
F123 **P123**	**16-bit data left rotate with carry flag (R9009) data**	**RCL** **PRCL**	D, n	Rotates the “n” bits in 17-bit area consisting of “D” plus the carry flag (R9009) data to the left.	5	○	○	○	○	○	○
F125 **P125**	**32-bit data right rotate**	**DROR** **PDROR**	D, n	Rotates the number of bits specified by “n” of the double words data (32 bits) specified by (D+1, D) to the right.	5	×	○	○	○	○	○
F126 **P126**	**32-bit data left rotate**	**DROL** **PDROL**	D, n	Rotates the number of bits specified by “n” of the double words data (32 bits) specified by (D+1, D) to the left.	5	×	○	○	○	○	○
F127 **P127**	**32-bit data right rotate with carry flag (R9009) data**	**DRCR** **PDRCR**	D, n	Rotates the number of bits specified by “n” of the double words data (32 bits) specified by (D+1, D) to the right together with carry flag (R9009) data.	5	×	○	○	○	○	○
F128 **P128**	**32-bit data left rotate with carry flag (R9009) data**	**DRCL** **PDRCL**	D, n	Rotates the number of bits specified by “n” of the double words data (32 bits) specified by (D+1, D) to the left together with carry flag (R9009) data.	5	×	○	○	○	○	○
Bit manipulation instructions											
F130 **P130**	**16-bit data bit set**	**BTS** **PBTS**	D, n	Sets the value of bit position “n” of the data of “D” to 1.	5	○	○	○	○	○	○
F131 **P131**	**16-bit data bit reset**	**BTR** **PBTR**	D, n	Sets the value of bit position “n” of the data of “D” to 0.	5	○	○	○	○	○	○
F132 **P132**	**16-bit data invert**	**BTI** **PBTI**	D, n	Inverts the value of bit position “n” of the data of “D”.	5	○	○	○	○	○	○
F133 **P133**	**16-bit data bit test**	**BTT** **PBTT**	D, n	Tests the value of bit position “n” of the data of “D” and outputs the result to R900B.	5	○	○	○	○	○	○
F135 **P135**	**Number of on (1) bits in 16-bit data**	**BCU** **PBCU**	S, D	Stores the number of on bits in the data of “S” in “D”.	5	○	○	○	○	○	○
F136 **P136**	**Number of on (1) bits in 32-bit data**	**DBCU** **PDBCU**	S, D	Stores the number of on bits in the data of (S+1, S) in “D”.	7	○	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

Num-ber	Name	Boo-lean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Basic function instruction											
F137	**Auxiliary timer (16-bit)**	**STMR**	S, D	Turns on the specified output and R900D after 0.01 s × set value.	5	○	○	○	○	○	○
Special instructions											
F138 **P138**	**Hours, min-utes and sec-onds to seconds data**	**HMSS** **PHMSS**	S, D	Converts the hour, minute and second data of (S+1, S) to seconds data, and the converted data is stored in (D+1, D).	5	△ *1	○	○	○	○	○
F139 **P139**	**Seconds to hours, minutes and seconds data**	**SHMS** **PSHMS**	S, D	Converts the seconds data of (S+1, S) to hour, minute and second data, and the converted data is stored in (D+1, D).	5	△ *1	○	○	○	○	○
F140 **P140**	**Carry flag (R9009) set**	**STC** **PSTC**	-	Turns on the carry flag (R9009).	1	○	○	○	○	○	○
F141 **P141**	**Carry flag (R9009) reset**	**CLC** **PCLC**	-	Turns off the carry flag (R9009).	1	○	○	○	○	○	○
F142 **P142**	**Watching dog timer update**	**WDT** **PWDT**	S	The time (allowable scan time for the system) of watching dog timer is changed to “S” × 0.1 (ms) for that scan.	3	×	×	×	×	×	○
F143 **P143**	**Partial I/O update**	**IORF** **PIORF**	D1, D2	Updates the I/O from the number specified by “D1” to the number specified by “D2”.	5	○	○	○	○	○	○
F144	**Serial data communica-tion control**	**TRNS**	S, n	The COM port received flag (R9038) is set to off to enable reception. Beginning at “S”, “n” bytes of the data registers are sent from the COM port.	5	○ *2	×	×	×	○	○
F145 **P145**	**Data send**	**SEND** **PSEND**	S1, S2, D, N	Sends the data to another station in the network (MEWNET). (via link unit)	9	×	×	×	×	○	○
F146 **P146**	**Data receive**	**RECV** **PRECV**	S1, S2, N, D	Receives the data to another station in the network (MEWNET). (via link unit)	9	×	×	×	×	○	○
F145 **P145**	**Data send**	**SEND**	S1, S2, D, N	Sends the data to the slave station as the MOD bus master. (via COM port)	9	×	○	△ *3	○	×	×
F146 **P146**	**Data receive**	**RECV**	S1, S2, N, D	Receives the data from the slave station as the MOD bus master. (via COM port)	9	×	○	△ *3	○	×	×
F145 **P145**	**Data send**	**SEND**	S1, S2, D, N	Sends the data to the slave station of the MOD bus master, type II.	9	×	○	△ *4	△ *4	×	×
F146 **P146**	**Data receive**	**RECV**	S1, S2, N, D	Receives the data from the slave station of the MOD bus master, type II.	9	×	○	△ *4	△ *4	×	×
F145 **P145**	**Data send**	**SEND**	S1, S2, D, N	Sends the data to the slave station as the MEWTOCOL master. (via COM port)	9	×	○	△ *3	△ *3	×	×
F146 **P146**	**Data receive**	**RECV**	S1, S2, N, D	Receives the data from the slave station as the MEWTOCOL master. (via COM port)	9	×	○	△ *3	△ *3	×	×
F147	**Printout**	**PR**	S, D	Converts the ASCII code data in the area starting with “S” for printing, and outputs it to the word external output relay WY specified by “D”.	5	○	○	○	○	○	○
F148 **P148**	**Self-diagnostic error set**	**ERR** **PERR**	n (n: k100 to K299)	Stores the self-diagnostic error number “n” in (DT9000), turns R9000 on, and turns on the ERROR LED.	3	○	○	○	○	○	○
F149 **P149**	**Message display**	**MSG** **PMSG**	S	Displays the character constant of “S” in the connected programming tool.	13	○	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

*1) The instruction is available for FP0 T32 (V2.3 or later) and FP-e.

*2) This instruction is available for FP0 V1.20 or later and FP-e.

*3) This instruction is available for FP-X V1.20 or later and FPΣ 32k type.

*4) This instruction is available for FP-X V2.50 or later and FPΣ V3.20 or later.s

Num-ber	Name	Boolean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F150 P150	**Data read from intelligent unit**	**READ PREAD**	S1, S2, n, D	Reads the data from the intelligent unit.	9	×	×	△ *3	×	○	○
F151 P151	**Data write into intelligent unit**	**WRT PWRT**	S1, S2, n, D	Writes the data into the intelligent unit.	9	×	×	△ *3	×	○	○
F152 P152	**Data read from MEWNET-F slave station**	**RMRD PRMRD**	S1, S2, n, D	Reads the data from the intelligent unit at the MEWNET-F (remote I/O) slave station.	9	×	×	×	×	○	○
F153 P153	**Data write into MEWNET-F slave station**	**RMWT PRMWT**	S1, S2, n, D	Writes the data into the intelligent unit at the MEWNET-F (remote I/O) slave station.	9	×	×	×	×	○	○
F155 P155	**Sampling**	**SMPL PSMPL**	-	Starts sampling data.	1	×	○	△ *5	△ *4	○	○
F156 P156	**Sampling trigger**	**STRG PSTRG**	-	When the trigger of this instruction turns on, the sampling trace stops.	1	×	○	△ *5	△ *4	○	○
F157 P157	**Time addition**	**CADD PCADD**	S1, S2, D	The time after (S2+1, S2) elapses from the time of (S1+2, S1+1, S1) is stored in (D+2, D+1, D).	9	△ *1	○	○	○	○	○
F158 P158	**Time subtraction**	**CSUB PCSUB**	S1, S2, D	The time that results from subtracting (S2+1, S2) from the time (S1+2, S1+1, S1) is stored in (D+2, D+1, D).	9	△ *1	○	○	○	○	○
F159 P159	**Serial port communication**	**MTRN PMTRN**	S, n, D	This is used to send data to an external device through the specified CPU COM port or MCU COM port.	7	×	○	○	○	△ *2	△ *2
F161 P161	**MCU serial port reception**	**MRCV PMRCV**	S, D1, D2	Data is received from external equipment via the COM port of the specified MCU.	7	×	×	×	×	△ *2	△ *2
BIN arithmetic instruction											
F160 P160	**Double word (32-bit) data square root**	**DSQR PDSQR**	S, D	$\sqrt{(S)} \rightarrow (D)$	7	×	○	○	○	○	○
High speed counter/Pulse output instruction for FP0, FP-e											
F0	**High-speed counter and Pulse output controls**	**MV**	S, DT9052	Performs high-speed counter and Pulse output controls according to the control code specified by “S”. The control code is stored in DT9052.	5	○					
1	**Change and read of the elapsed value of high-speed counter and Pulse output**	**DMV**	S, DT9044	Transfers (S+1, S) to high-speed counter and Pulse output elapsed value area.	7	○					
			DT9044, D	Transfers value in high-speed counter and Pulse output elapsed value area to (D+1, D).	7	○					
F166	**High-speed counter output set (with channel specification)**	**HC1S**	n, S, Yn	Turns output Yn on when the elapsed value of the built-in high-speed counter reaches the target value of (S+1, S).	11	○					

○ : Available, × : Not available, △ : Not available partially

*1) The instruction is available for FP0 T32 (V2.3 or later) and FP-e.

*2) The instruction is available for FP2/FP2SH Ver. 1.5 or later, and the pulse execution type can be specified. FP10SH cannot be used.

*3) This instruction is available for FPΣ Ver. 2.0 or later.

*4) This instruction is only available for FP-X Ver.2.0 or later.

*5) This instruction is available for FPΣ Ver. 3.10 or later.

Number	Name	Boolean	Operand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F167	**High-speed counter output reset (with channel specification)**	**HC1R**	n, S, Yn	Turns output Yn off when the elapsed value of the built-in high-speed counter reaches the target value of (S+1, S).	11	○					
F168	**Positioning control (with channel specification)**	**SPD1**	S, n	Outputs a positioning pulse from the specified output (Y0 or Y1) according to the contents of the data table beginning at "S".	5	○					
F169	**Pulse output (with channel specification)**	**PLS**	S, n	Outputs a pulse from the specified output (Y0 or Y1) according to the contents of the data table beginning at "S".	5	○					
F170	**PWM output (with channel specification)**	**PWM**	S, n	Performs PWM output from the specified output (Y0 or Y1) according to the contents of the data table beginning at "S".	5	○					
High speed counter/Pulse output instruction for FP0R											
F0	**High-speed counter and Pulse output controls**	**MV**	S, DT90052	Performs high-speed counter and Pulse output controls according to the control code specified by "S". The control code is stored in DT90052.	5		○				
F1	**Change and read of the elapsed value of high-speed counter and Pulse output**	**DMV**	S, DT90300	Transfers (S+1, S) to high-speed counter and Pulse output elapsed value area (DT90045, DT90044).	7		○				
			DT90300, D	Transfers value in high-speed counter and Pulse output elapsed value area (DT90045, DT90044) to (D+1, D).	7		○				
F165	**Cam control**	**CAM0**	S	Controls cam operation (on/off patterns of each cam output) according to the elapsed value of the high-speed counter.	3		○				
F166	**Target value much on (with channel specification) (High-speed counter control/Pulse output control)**	**HC1S**	n, S, D	Turns output Yn on when the elapsed value of the high-speed counter or pulse output reaches the target value of (S+1, S).	11		○				
F167	**Target value much off (with channel specification) (High-speed counter control/Pulse output control)**	**HC1R**	n, S, D	Turns output Yn off when the elapsed value of the high-speed counter or pulse output reaches the target value of (S+1, S).	11		○				
F171	**Pulse output (JOG positioning type 0/1) (Trapezoidal control)**	**SPDH**	S, n	Positioning pulses are output from the specified channel, in accordance with the contents of the data table that starts with S.	5		○				
F172	**Pulse output (JOG operation 0 and 1)**	**PLSH**	S, n	Pulse strings are output from the specified output, in accordance with the contents of the data table that starts with S.	5		○				
F173	**PWM output (with channel specification)**	**PWMH**	S, n	PWM output is output from the specified output, in accordance with the contents of the data table that starts with S.	5		○				

Num-ber	Name	Boolean	Operand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F174	**Pulse output (Selectable data table control operation)**	**SP0H**	S, n	Outputs the pulses from the specified channel according to the data table specified by S.	5		○				
F175	**Pulse output (Linear interpolation)**	**SPSH**	S, n	Pulses are output from channel, in accordance with the designated data table, so that the path to the target position forms a straight line.	5		○				
F176	**Pulse output (Circular interpolation)**	**SPCH**	S, n	Pulses are output from channel, in accordance with the designated data table, so that the path to the target position forms an arc.	5		×				
F177	**Pulse output (Home return)**	**HOME**	S, n	Performs the home return according to the specified data table.	7		○				
F178	**Input pulse measurement (No. of pulses, cycle for input pulses)**	**PLSM**	S1, S2, D	Measures the number of pulses and cycle of pulses to be input to the high-speed counter of the specified channel.	5		○				

Number	Name	Boolean	Operand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
High speed counter/Pulse output instruction for FPΣ/FP-X											
F0	**High-speed counter and Pulse output controls**	**MV**	S, DT90052	Performs high-speed counter and Pulse output controls according to the control code specified by “S”. The control code is stored in DT90052.	5			○	○		
F1	**Change and read of the elapsed value of high-speed counter and Pulse output**	**DMV**	FPΣ: S, DT90044 FP-X: S, DT90300	Transfers (S+1, S) to high-speed counter and Pulse output elapsed value area (DT90045, DT90044).	7			○	○		
			FPΣ: DT90044, D FP-X: DT90300, D	Transfers value in high-speed counter and Pulse output elapsed value area (DT90045, DT90044) to (D+1, D).	7			○	○		
F166	**Target value much on (with channel specification)**	**HC1S**	n, S, D	Turns output Yn on when the elapsed value of the built-in high-speed counter reaches the target value of (S+1, S).	11			○	○		
F167	**Target value much off (with channel specification)**	**HC1R**	n, S, D	Turns output Yn off when the elapsed value of the built-in high-speed counter reaches the target value of (S+1, S).	11			○	○		
F171	**Pulse output (with channel specification) (Trapezoidal control and home return)**	**SPDH**	S, n	Positioning pulses are output from the specified channel, in accordance with the contents of the data table that starts with S.	5			○	○		
F172	**Pulse output (with channel specification) (JOG operation)**	**PLSH**	S, n	Pulse strings are output from the specified output, in accordance with the contents of the data table that starts with S.	5			○	○		
F173	**PWM output (with channel specification)**	**PWMH**	S, n	PWM output is output from the specified output, in accordance with the contents of the data table that starts with S.	5			○	○		
F174	**Pulse output (with channel specification) (Selectable data table control operation)**	**SP0H**	S, n	Outputs the pulses from the specified channel according to the data table specified by S.	5			○	○		
F175	**Pulse output (Linear interpolation)**	**SPSH**	S, n	Pulses are output from channel, in accordance with the designated data table, so that the path to the target position forms a straight line.	5			△ *2	○		
F176	**Pulse output (Circular interpolation)**	**SPCH**	S, n	Pulses are output from channel, in accordance with the designated data table, so that the path to the target position forms an arc.	5			△ *2	×		

○ : Available, × : Not available, △ : Not available partially

*1) The elapsed value area differs depending on used channels.

*2) This instruction is available for FPΣ C32T2, C28P2, C32T2H and C28P2H.

Num -ber	Name	Boolean	Ope- rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Screen display instructions											
F180	**FP-e screen display registration**	**SCR**	S1, S2, S3, S4	Register the screen displayed on the FP-e.	9	△ *1	×	×	×	×	×
F181	**FP-e screen display switching**	**DSP**	S	Specify the screen to be displayed on the FP-e.	3	△ *1	×	×	×	×	×
Basic function instruction											
F182	**Time constant processing**	**FILTR**	S1, S2, S3, D	Executes the filter processing for the specified input.	9	×	○	△ *2	△ *3	×	×
F183	**Auxiliary timer (32-bit)**	**DSTM**	S, D	Turn on the specified output and R900D after 0.01 s. × set value.	7	○	○	○	○	○	△ *4
Data transfer instructions											
F190 P190	**Three 16-bit data move**	**MV3 PMV3**	S1, S2, S3, D	(S1)→(D), (S2)→(D+1), (S3)→(D+2)	10	×	○	○	○	○	○
F191 P191	**Three 32-bit data move**	**DMV3 PDMV3**	S1, S2, S3, D	(S1+1, S1)→(D+1, D), (S2+1, S2)→(D+3, D+2), (S3+1, S3)→(D+5, D+4)	16	×	○	○	○	○	○
Logic operation instructions											
F215 P215	**32-bit data AND**	**DAND PDAND**	S1, S2, D	(S1+1, S1) AND (S2+1, S2)→(D+1, D)	7	×	○	○	○	○	○
F216 P216	**32-bit data OR**	**DOR PDOR**	S1, S2, D	(S1+1, S1) OR (S2+1, S2)→(D+1, D)	12	×	○	○	○	○	○
F217 P217	**32-bit data XOR**	**DXOR PDXOR**	S1, S2, D	{(S1+1, S1) AND (S2+1, S2)} OR {(S1+1, S1) AND (S2+1, S2)}→(D+1, D)	12	×	○	○	○	○	○
F218 P218	**32-bit data XNR**	**DXNR PDXNR**	S1, S2, D	{(S1+1, S1) AND (S2+1, S2)} OR {(S1+1, S1) AND (S2+1, S2)}→(D+1, D)	12	×	○	○	○	○	○
F219 P219	**Double word (32-bit) data unites**	**DUNI PDUNI**	S1, S2, S3, D	{(S1+1, S1) AND (S3+1, S3)} OR {(S2+1, S2) AND (S3+1, S3)}→(D+1, D)	16	×	○	○	○	○	○
Data conversion instructions											
F230 P230	**Time data → second conversion**	**TMSEC PTMSEC**	S, D	The specified time data (a date and time) is changed to the second data.	6	×	○	△ *5	△ *6	△ *7	△ *7
F231 P231	**Second data→ time conversion**	**SECTM PSECTM**	S, D	The specified second data is changed into time data (a date and time).	6	×	○	△ *5	△ *6	△ *7	△ *7

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is available for FP-e only.

*2) This instruction is available for FPΣ Ver. 3.10 or later.

*3) This instruction is only available for FP-X Ver.2.0 or later.

*4) This instruction is available for FP10SH Ver. 3.10 or later.

*5) This instruction is available for FPΣ 32k type.

*6) This instruction is available for FP-X Ver. 1.13 or later.

*7) This instruction is available for FP2/FP2SH Ver. 1.5 or later.FP10SH cannot be used.

Number	Name	Boolean	Operand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F235 P235	**16-bit binary data → Gray code conversion**	**GRY PGRY**	S, D	Converts the 16-bit binary data of “S” to gray codes, and the converted result is stored in the “D”.	6	×	○	○	○	○	○
F236 P236	**32-bit binary data → Gray code conversion**	**DGRY PDGRY**	S, D	Converts the 32-bit binary data of (S+1, S) to gray code, and the converted result is stored in the (D+1, D).	8	×	○	○	○	○	○
F237 P237	**16-bit gray code → binary data conversion**	**GBIN PGBIN**	S, D	Converts the gray codes of “S” to binary data, and the converted result is stored in the “D”.	6	×	○	○	○	○	○
F238 P238	**32-bit gray code → binary data conversion**	**DGBIN PDGBIN**	S, D	Converts the gray codes of (S+1, S) to binary data, and the converted result is stored in the (D+1, D).	8	×	○	○	○	○	○
F240 P240	**Bit line to bit column conversion**	**COLM PCOLM**	S, n, D	The values of bits 0 to 15 of “S” are stored in bit “n” of (D to DC+15).	8	×	○	○	○	○	○
F241 P241	**Bit column to bit line conversion**	**LINE PLINE**	S, n, D	The values of bit “n” of (S) to (S+15) are stored in bits 0 to 15 of “D”.	8	×	○	○	○	○	○
F250	**Binary data → ASCII conversion**	**BTOA**	S1, S2, n, D	Converts multiple binary data to multiple ASCII data.	12	×	○	△ *1	○	×	×
F251	**ASCII → binary data conversion**	**ATOB**	S1, S2, n, D	Converts multiple ASCII data to multiple binary data.	12	×	○	△ *1	○	×	×
F252	**ASCII data check**	**ACHK**	S1, S2, n	Checks the ASCII data strings to be used in F251 (ATOB) instruction.	10	×	○	△ *2	△ *3	×	×
Character strings instructions											
F257 P257	**Comparing character strings**	**SCMP**	S1, S2	These instructions compare two specified character strings and output the judgment results to a special internal relay.	10	×	○	○	○	○	○
F258 P258	**Character string coupling**	**SADD**	S1, S2, D	These instructions couple one character string with another.	12	×	○	○	○	○	○
F259 P259	**Number of characters in a character string**	**LEN**	S, D	These instructions determine the number of characters in a character string.	6	×	○	○	○	○	○
F260 P260	**Search for character string**	**SSRC**	S1, S2, D	The specified character is searched in a character string.	10	×	○	○	○	○	○
F261 P261	**Retrieving data from character strings (right side)**	**RIGHT**	S1, S2, D	These instructions retrieve a specified number of characters from the right side of the character string.	8	×	○	○	○	○	○
F262 P262	**Retrieving data from character strings (left side)**	**LEFT**	S1, S2, D	These instructions retrieve a specified number of characters from the left side of the character string.	8	×	○	○	○	○	○
F263 P263	**Retrieving a character string from a character string**	**MIDR**	S1, S2, S3, D	These instructions retrieve a character string consisting of a specified number of characters from the specified position in the character string.	10	×	○	○	○	○	○
F264 P264	**Writing a character string to a character string**	**MIDW**	S1, S2, D, n	These instructions write a specified number of characters from a character string to a specified position in the character string.	12	×	○	○	○	○	○
F265 P265	**Replacing character strings**	**SREP**	S, D, p, n	A specified number of characters in a character string are rewritten, starting from a specified position in the character string.	12	×	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is available for FPΣ 32k type.

*2) This instruction is available for FPΣ Ver. 3.10 or later.

*3) This instruction is only available for FP-X Ver.2.0 or later.

Num-ber	Name	Boolean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Integer type data processing instructions											
F270 P270	**Maximum value (word data (16-bit))**	**MAX PMAX**	S1, S2, D	Searches the maximum value in the word data table between the “S1” and “S2”, and stores it in the “D”. The address relative to “S1” is stored in “D+1”.	8	△ *1	○	○	○	○	○
F271 P271	**Maximum value (double word data (32-bit))**	**DMAX PDMAX**	S1, S2, D	Searches for the maximum value in the double word data table between the area selected with “S1” and “S2”, and stores it in the “D”. The address relative to “S1” is stored in “D+2”.	8	△ *1	○	○	○	○	○
F272 P272	**Minimum value (word data (16-bit))**	**MIN PMIN**	S1, S2, D	Searches for the minimum value in the word data table between the area selected with “S1” and “S2”, and stores it in the “D”. The address relative to “S1” is stored in “D+1”.	8	△ *1	○	○	○	○	○
F273 P273	**Minimum value (double word data (32-bit))**	**DMIN PDMIN**	S1, S2, D	Searches for the minimum value in the double word data table between the area selected with “S1” and “S2”, and stores it in the “D”. The address relative to “S1” is stored in “D+2”.	8	△ *1	○	○	○	○	○
F275 P275	**Total and mean values (word data (16-bit))**	**MEAN PMEAN**	S1, S2, D	The total value and the mean value of the word data with sign from the area selected with “S1” to “S2” are obtained and stored in the “D”.	8	△ *1	○	○	○	○	○
F276 P276	**Total and mean values (double word data (32-bit))**	**DMEAN PDMEAN**	S1, S2, D	The total value and the mean value of the double word data with sign from the area selected with “S1” to “S2” are obtained and stored in the “D”.	8	△ *1	○	○	○	○	○
F277 P277	**Sort (word data (16-bit))**	**SORT PSORT**	S1, S2, S3	The word data with sign from the area specified by “S1” to “S2” are sorted in ascending order (the smallest word is first) or descending order (the largest word is first).	8	△ *1	○	○	○	○	○
F278 P278	**Sort (double word data (32-bit))**	**DSORT PDSORT**	S1, S2, S3	The double word data with sign from the area specified by “S1” to “S2” are sorted in ascending order (the smallest word is first) or descending order (the largest word is first).	8	△ *1	○	○	○	○	○
F282 P282	**Scaling of 16-bit data**	**SCAL PSCAL**	S1, S2, D	The output value Y is found for the input value X by performing scaling for the given data table.	8	△ *1	○	○	○	○	○
F283 P283	**Scaling of 32-bit data**	**DSCAL PDSCAL**	S1, S2, D	The output value Y is found for the input value X by performing scaling for the given data table.	10	×	○	○	○	○	○
F284 P284	**Inclination output of 16-bit data**	**RAMP**	S1, S2, S3, D	Executes the linear output for the specified time from the specified initial value to the target value.	10	×	○	△ *2	△ *2	×	×
Integer type non-linear function instructions											
F285 P285	**Upper and lower limit control (16-bit data)**	**LIMT PLIMT**	S1, S2, S3, D	When S1>S3, S1→D When S1<S3, S2→D When S1<or = S3<or = S2, S3→D	10	△ *1	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is only available for FP-e Ver.1.2 or later.

*2) This instruction is only available for FP-X Ver.2.0 or later, and FPΣ Ver. 3.10 or later.

Num-ber	Name	Boolean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F286 **P286**	**Upper and lower limit control (32-bit data)**	**DLIMT** **PDLIMT**	S1, S2, S3, D	When (S1+1, S1)>(S3+1, S3), (S1+1, S1)→(D+1, D) When (S2+1, S2)<(S3+1, S3), (S2+1, S2)→(D+1, D) When (S1+1, S1)<or = (S3+1, S3)<or = (S2+1, S2), (S3+1, S3)→(D+1, D)	16	△ *1	○	○	○	○	○
F287 **P287**	**Deadband control (16-bit data)**	**BAND** **PBAND**	S1, S2, S3, D	When S1>S3, S3–S1→D When S2<S3, S3–S2→D When S1<or = S3<or = S2, 0→D	10	△ *1	○	○	○	○	○
F288 **P288**	**Deadband control (32-bit data)**	**DBAND** **PDBAND**	S1, S2, S3, D	When (S1+1, S1)>(S3+1, S3), (S3+1, S3)–(S1+1, S1)→(D+1, D) When (S2+1, S2)<(S3+1, S3), (S3+1, S3)–(S2+1, S2)→(D+1, D) When (S1+1, S1)<or = (S3+1, S3)<or = (S2+1, S2),0→(D+1, D)	16	△ *1	○	○	○	○	○
F289 **P289**	**Zone control (16-bit data)**	**ZONE** **PZONE**	S1, S2, S3, D	When S3<0, S3+S1→D When S3=0, 0→D When S3>0, S3+S2→D	10	△ *1	○	○	○	○	○
F290 **P290**	**Zone control (32-bit data)**	**DZONE** **PDZONE**	S1, S2, S3, D	When (S3+1, S3)<0, (S3+1, S3)+(S1+1, S1)→(D+1, D) When (S3+1, S3)=0, 0→(D+1, D) When (S3+1, S3)>0, (S3+1, S3)+(S2+1, S2)→(D+1, D)	16	△ *1	○	○	○	○	○
BCD type real number operation instructions											
F300 **P300**	**BCD type sine operation**	**BSIN** **PBSIN**	S, D	SIN(S1+1, S1)→(D+1, D)	6	×	×	×	×	○	○
F301 **P301**	**BCD type cosine operation**	**BCOS** **PBCOS**	S, D	COS(S1+1, S1)→(D+1, D)	6	×	×	×	×	○	○
F302 **P302**	**BCD type tangent operation**	**BTAN** **PBTAN**	S, D	TAN(S1+1, S1)→(D+1, D)	6	×	×	×	×	○	○
F303 **P303**	**BCD type arcsine operation**	**BASIN** **PBASIN**	S, D	SIN^{-1}(S1+1, S1)→(D+1, D)	6	×	×	×	×	○	○
F304 **P304**	**BCD type arccosine operation**	**BACOS** **PBACOS**	S, D	COS^{-1}(S1+1, S1)→(D+1, D)	6	×	×	×	×	○	○
F305 **P305**	**BCD type arctangent operation**	**BATAN** **PBATAN**	S, D	TAN^{-1}(S1+1, S1)→(D+1, D)	6	×	×	×	×	○	○
Floating-point type real number operation instructions											
F309 **P309**	**Floating-point type data move**	**FMV** **PFMV**	S, D	(S+1, S)→(D+1, D)	8	△ *2	○	○	○	○	○
F310 **P310**	**Floating-point type data addition**	**F+** **PF+**	S1, S2, D	(S1+1, S1)+(S2+1, S2)→(D+1, D)	14	△ *2	○	○	○	○	○
F311 **P311**	**Floating-point type data subtraction**	**F-** **PF-**	S1, S2, D	(S1+1, S1)–(S2+1, S2)→(D+1, D)	14	△ *2	○	○	○	○	○
F312 **P312**	**Floating-point type data multiplication**	**F*** **PF***	S1, S2, D	(S1+1, S1)×(S2+1, S2)→(D+1, D)	14	△ *2	○	○	○	○	○
F313 **P313**	**Floating-point type data division**	**F%** **PF%**	S1, S2, D	(S1+1, S1)÷(S2+1, S2)→(D+1, D)	14	△ *2	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is only available for FP-e Ver.1.2 or later.

*2) This instruction is available for FP-e Ver.1.21 or later, and FP0 V2.1 or later.

Number	Name	Boolean	Operand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F314 P314	**Floating-point type data sine operation**	**SIN PSIN**	S, D	SIN(S+1, S)→(D+1, D)	10	△ *1	○	○	○	○	○
F315 P315	**Floating-point type data cosine operation**	**COS PCOS**	S, D	COS(S+1, S)→(D+1, D)	10	△ *1	○	○	○	○	○
F316 P316	**Floating-point type data tangent operation**	**TAN PTAN**	S, D	TAN(S+1, S)→(D+1, D)	10	△ *1	○	○	○	○	○
F317 P317	**Floating-point type data arcsine operation**	**ASIN PASIN**	S, D	SIN^{-1}(S+1, S)→(D+1, D)	10	△ *1	○	○	○	○	○
F318 P318	**Floating-point type data arccosine operation**	**ACOS PACOS**	S, D	COS^{-1}(S+1, S)→(D+1, D)	10	△ *1	○	○	○	○	○
F319 P319	**Floating-point type data arctangent operation**	**ATAN PATAN**	S, D	TAN^{-1}(S+1, S)→(D+1, D)	10	△ *1	○	○	○	○	○
F320 P320	**Floating-point type data natural logarithm**	**LN PLN**	S, D	LN(S+1, S)→(D+1, D)	10	△ *1	○	○	○	○	○
F321 P321	**Floating-point type data exponent**	**EXP PEXP**	S, D	EXP(S+1, S)→(D+1, D)	10	△ *1	○	○	○	○	○
F322 P322	**Floating-point type data logarithm**	**LOG PLOG**	S, D	LOG(S+1, S)→(D+1, D)	10	△ *1	○	○	○	○	○
F323 P323	**Floating-point type data power**	**PWR PPWR**	S1, S2, D	(S1+1, S1) ^ (S2+1, S2)→(D+1, D)	14	△ *1	○	○	○	○	○
F324 P324	**Floating-point type data square root**	**FSQR PFSQR**	S, D	$\sqrt{(S+1, S)}$→(D+1, D)	10	△ *1	○	○	○	○	○
F325 P325	**16-bit integer data to floating-point type data conversion**	**FLT PFLT**	S, D	Converts the 16-bit integer data with sign specified by “S” to real number data, and the converted data is stored in “D”.	6	△ *1	○	○	○	○	○
F326 P326	**32-bit integer data to floating-point type data conversion**	**DFLT PDFLT**	S, D	Converts the 32-bit integer data with sign specified by (S+1, S) to real number data, and the converted data is stored in (D+1, D).	8	△ *1	○	○	○	○	○
F327 P327	**Floating-point type data to 16-bit integer conversion (the largest integer not exceeding the floating-point type data)**	**INT PINT**	S, D	Converts real number data specified by (S+1, S) to the 16-bit integer data with sign (the largest integer not exceeding the floating-point data), and the converted data is stored in “D”.	8	△ *1	○	○	○	○	○
F328 P328	**Floating-point type data to 32-bit integer conversion (the largest integer not exceeding the floating-point type data)**	**DINT PDINT**	S, D	Converts real number data specified by (S+1, S) to the 32-bit integer data with sign (the largest integer not exceeding the floating-point data), and the converted data is stored in (D+1, D).	8	△ *1	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is available for FP-e Ver.1.21 or later, and FP0 V2.1 or later.

Number	Name	Boolean	Operand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F329 P329	**Floating-point type data to 16-bit integer conversion (rounding the first decimal point down to integer)**	**FIX PFIX**	S, D	Converts real number data specified by (S+1, S) to the 16-bit integer data with sign (rounding the first decimal point down), and the converted data is stored in “D”.	8	△ *1	○	○	○	○	○
F330 P330	**Floating-point type data to 32-bit integer conversion (rounding the first decimal point down to integer)**	**DFIX PDFIX**	S, D	Converts real number data specified by (S+1, S) to the 32-bit integer data with sign (rounding the first decimal point down), and the converted data is stored in (D+1, D).	8	△ *1	○	○	○	○	○
F331 P331	**Floating-point type data to 16-bit integer conversion (rounding the first decimal point off to integer)**	**ROFF PROFF**	S, D	Converts real number data specified by (S+1, S) to the 16-bit integer data with sign (rounding the first decimal point off), and the converted data is stored in “D”.	8	△ *1	○	○	○	○	○
F332 P332	**Floating-point type data to 32-bit integer conversion (rounding the first decimal point off to integer)**	**DROFF PDROFF**	S, D	Converts real number data specified by (S+1, S) to the 32-bit integer data with sign (rounding the first decimal point off), and the converted data is stored in (D+1, D).	8	△ *1	○	○	○	○	○
F333 P333	**Floating-point type data rounding the first decimal point down**	**FINT PFINT**	S, D	The decimal part of the real number data specified in (S+1, S) is rounded down, and the result is stored in (D+1, D).	8	△ *1	○	○	○	○	○
F334 P334	**Floating-point type data rounding the first decimal point off**	**FRINT PFRINT**	S, D	The decimal part of the real number data stored in (S+1, S) is rounded off, and the result is stored in (D+1, D).	8	△ *1	○	○	○	○	○
F335 P335	**Floating-point type data sign changes**	**F+/- PF+/-**	S, D	The real number data stored in (S+1, S) is changed the sign, and the result is stored in (D+1, D).	8	△ *1	○	○	○	○	○
F336 P336	**Floating-point type data absolute**	**FABS PFABS**	S, D	Takes the absolute value of real number data specified by (S+1, S), and the result (absolute value) is stored in (D+1, D).	8	△ *1	○	○	○	○	○
F337 P337	**Floating-point type data degree → radian**	**RAD PRAD**	S, D	The data in degrees of an angle specified in (S+1, S) is converted to radians (real number data), and the result is stored in (D+1, D).	8	△ *1	○	○	○	○	○
F338 P338	**Floating-point type data radian → degree**	**DEG PDEG**	S, D	The angle data in radians (real number data) specified in (S+1, S) is converted to angle data in degrees, and the result is stored in (D+1, D).	8	△ *1	○	○	○	○	○
Floating-point type real number data processing instructions											
F345 P345	**Floating-point type data compare**	**FCMP PFCMP**	S1, S2	(S1+1, S1)>(S2+1, S2)→ R900A: on (S1+1, S1)=(S2+1, S2)→ R900B on (S1+1, S1)<(S2+1, S2)→ R900C: on	10	×	○	○	○	○	○
F346 P346	**Floating-point type data band compare**	**FWIN PFWIN**	S1, S2, S3	(S1+1, S1)>(S3+1, S3)→ R900A: on (S2+1, S2)<or =(S1+1, S1)<or =(S3+1, S3) → R900B on (S1+1, S1)<(S2+1, S2)→ R900C: on	14	×	○	○	○	○	○

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is available for FP-e Ver.1.21 or later, and FP0 V2.1 or later.

Num-ber	Name	Boolean	Ope-rand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
F347 P347	**Floating-point type data upper and lower limit control**	**FLIMT PFLIMT**	S1, S2, S3, D	When (S1+1, S1)>(S3+1, S3), (S1+1, S1) →(D+1, D) When (S2+1, S2)<(S3+1, S3), (S2+1, S2) → (D+1, D) When (S1+1, S1)<or = (S3+1, S3)<or =(S2+1, S2), (S3+1, S3)→(D+1, D)	17	×	○	○	○	○	○
F348 P348	**Floating-point type data dead-band control**	**FBAND PFBAND**	S1, S2, S3, D	When (S1+1, S1)>(S3+1, S3), (S3+1, S3)–(S1+1, S1)→(D+1, D) When (S2+1, S2)<(S3+1, S3), (S3+1, S3)–(S2+1, S2)→ (D+1, D) When (S1+1, S1)<or = (S3+1, S3)<or =(S2+1, S2), 0.0→(D+1, D)	17	×	○	○	○	○	○
F349 P349	**Floating-point type data zone control**	**FZONE PFZONE**	S1, S2, S3, D	When (S3+1, S3)<0.0, (S3+1, S3)+(S1+1, S1)→(D+1, D) When (S3+1, S3)=0.0, 0.0→ (D+1, D) When (S3+1, S3)>0.0, (S3+1, S3)+(S2+1, S2) →(D+1, D)	17	×	○	○	○	○	○
F350 P350	**Floating-point type data maxi-mum value**	**FMAX PFMAX**	S1, S2, D	Searches the maximum value in the real number data table between the area selected with “S1” and “S2”, and stores it in the (D+1, D). The address relative to “S1” is stored in (D+2).	8	×	×	×	×	○	○
F351 P351	**Floating-point type data mini-mum value**	**FMIN PFMIN**	S1, S2, D	Searches the minimum value in the real number data table between the area selected with “S1” and “S2”, and stores it in the (D+1, D). The address relative to “S1” is stored in (D+2).	8	×	×	×	×	○	○
F352 P352	**Floating-point type data total and mean values**	**FMEAN PFMEAN**	S1, S2, D	The total value and the mean value of the real number data from the area selected with “S1” to “S2” are obtained. The total value is stored in the (D+1, D) and the mean value is stored in the (D+3, D+2).	8	×	×	×	×	○	○
F353 P353	**Floating-point type data sort**	**FSORT PFSORT**	S1, S2, S3	The real number data from the area specified by “S1” to “S2” are stored in ascending order (the smallest word is first) or descending order (the largest word is first).	8	×	×	×	×	○	○
F354 P354	**Scaling of real number data**	**FSCAL PFSCAL**	S1, S2, D	Scaling (linearization) on a real number data table is performed, and the output (Y) to an input value (X) is calculated.	12	×	○	△ *1	△ *2	△ *3	△ *3

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is available for FPΣ 32k type.

*2) This instruction is available for FP-X Ver. 1.13 or later.

*3) This instruction is available for FP2/FP2SH Ver. 1.5 or later. FP10SH cannot be used.

Number	Name	Boolean	Operand	Description	Steps	FP0/FP-e	FP0R	FPΣ	FP-X	FP2	FP2SH/FP10SH
Time series processing instruction											
F355	**PID processing**	**PID**	S	PID processing is performed depending on the control value (mode and parameter) specified by (S to S+2) and (S+4 to S+10), and the result is stored in the (S+3).	4	△ *1	○	○	○	○	○
F356	**Easy PID**	**EZPID**	S1, S2, S3, S4	Temperature control (PID) can be easily performed using the image of a temperature controller.	10	×	○	△ *2	△ *2	×	×
Compare instructions											
F373 P373	**16-bit data revision detection**	**DTR PDTR**	S, D	If the data in the 16-bit area specified by "S" has changed since the previous execution, internal relay R9009 (carry flag) will turn on. "D" is used to store the data of the previous execution.	6	×	○	○	○	○	○
F374 P374	**32-bit data revision detection**	**DDTR PDDTR**	S, D	If the data in the 32-bit area specified by (S+1, S) has changed since the previous execution, internal relay R9009 (carry flag) will turn on. (D+1, D) is used to store the data of the previous execution.	6	×	○	○	○	○	○
Index register bank processing instructions											
F410 P410	**Setting the index register bank number**	**SETB PSETB**	n	Index register (I0 to ID) bank number change over.	4	×	×	×	×	×	○
F411 P411	**Changing the index register bank number**	**CHGB PCHGB**	n	Index register (I0 to ID) bank number change over with remembering preceding bank number.	4	×	×	×	×	×	○
F412 P412	**Restoring the index register bank number**	**POPB PPOPB**	-	Changes index register (I0 to ID) bank number back to the bank before F411 (CHGB)/P411 (PCHGB) instruction.	2	×	×	×	×	×	○
File register bank processing instructions											
F414 P414	**Setting the file register bank number**	**SBFL PSBFL**	n	File register bank number change over.	4	×	×	×	×	×	△ *3
F415 P415	**Changing the file register bank number**	**CBFL PCBFL**	n	File register bank number change over with remembering preceding bank number.	4	×	×	×	×	×	△ *3
F416 P416	**Restoring the file register bank number**	**PBFL PPBFL**	-	Changes file register bank number back to the bank before F415 (CBFL)/P415 (PCBFL) instruction.	2	×	×	×	×	×	△ *3

○ : Available, × : Not available, △ : Not available partially

*1) This instruction is available for FP0 (V2.1 or later) only.

*2) This instruction is available for FP-X V.1.20 or later, and FPΣ 32k type.

*3) This instruction is not available for FP10SH.

11.4 Table of Error codes

■ Difference in ERROR display

There are differences in the way errors are displayed depending on the model.

Model	Display		Display method
FP1,FP-M,FP2,FP3,FP10SH	LED	ERROR.	Continually lit
FPΣ,FP0, FP0R, FP-X	LED	ERROR/ALARM	Flashes/continually lit
FP-e	Screen display	ERR.	Continually lit

■ Error Confirmation When ERROR Turns ON

When the “ERROR” on the control unit (CPU unit) turns on or flashes, a self-diagnostic error or syntax check error has occurred. Confirm the contents of the error and take the appropriate steps.

-Error Confirmation Method

Procedure:1.Use the programming tool software to call up the error code.
By executing the “STATUS DISPLAY”, the error code and content of error are displayed.
2.Check the error contents in the table of error codes using the error code ascertained above.

-Syntax check error

This is an error detected by the total check function when there is a syntax error or incorrect setting written in the program. When the mode selector is switched to the RUN mode, the total check function automatically activates and eliminates the possibility of incorrect operation from syntax errors in the program.

When a syntax check error is detected

-ERROR turns on or flashes.
-Operation will not begin even after switching to the RUN mode.
-Remote operation cannot be used to change to RUN mode.

Clearing a syntax check error

By changing to the PROG. mode, the error will clear and the ERROR will turn off.

Steps to take for syntax error

Change to the PROG. mode, and then execute the total check function while online mode with the programming tool connected. This will call up the content of error and the address where the error occurred.
Correct the program while referring to the content of error.

-Self-diagnostic Error

This error occurs when the control unit (CPU unit) self-diagnostic function detects the occurrence of an abnormality in the system. The self-diagnostic function monitors the memory abnormal detection, I/O abnormal detection, and other devices.

When a self-diagnostic error occurs

- The ERROR turns on or flashes.
- The operation of the control unit (CPU unit) might stop depending on the content of error and the system register setting.
- The error codes will be stored in the special data register DT9000(DT90000).
- In the case of operation error, the error address will be stored in the DT9017(DT90017) and DT9018(DT90018).

Clearing the self-diagnostic error

At the “STATUS DISPLAY”, execute the “error clear”. Error codes 43 and higher can be cleared.

-You can use the initialize/test switch to clear an error. However, this will also clear the contents of operation memory.

-Errors can also be cleared by turning off and on the power while in the PROG. mode.
However, the contents of operation memory, not stored with the hold type data, will also be cleared.

-The error can also be cleared depending on the self-diagnostic error set instruction F148(ERR).

Steps to take for self-diagnostic error

The steps to be taken will differ depending on the error contents. For more details, use the error code obtained above and consult the table of self-diagnostic error codes.

■ MEWTOCOL-COM Transmission Errors

These are error codes from a PC or other computer device that occur during an abnormal response when communicating with a PLC using MEWTOCOL-COM.

11.4.1 Table of Syntax Check Error

Error code	Name	Operation status	Description and steps to take	FP-e	FP0	FP0R	FP Σ	FP-X	FP2	FP2SH	FP10SH
E1	**Syntax error**	Stops	A program with a syntax error has been written. ⇒ Change to PROG. mode and correct the error.	A	A	A	A	A	A	A	A
E2 (Note)	**Duplicated output error**	Stops	Two or more OT(Out) instructions and KP(Keep) instructions are programmed using the same relay. Also occurs when using the same timer/counter number. ⇒ Change to PROG. mode and correct the program so that one relay is not used for two or more OT instructions. Or, set the duplicated output to “enable” in system register 20. A timer/counter instruction double definition error will be detected even if double output permission has been selected.	A	A	A	A	A	A	A	A
E3	**Not paired error**	Stops	For instructions which must be used in a pair such as jump (JP and LBL), one instruction is either missing or in an incorrect position. ⇒ Change to PROG. mode and enter the two instructions which must be used in a pair in the correct positions.	A	A	A	A	A	A	A	A
E4	**Parameter mismatch error**	Stops	An instruction has been written which does not agree with system register settings. For example, the number setting in a program does not agree with the timer/counter range setting. ⇒ Change to PROG. mode, check the system register settings, and change so that the settings and the instruction agree.	A	A	A	A	A	A	A	A
E5 (Note)	**Program area error**	Stops	An instruction which must be written in a specific area (main program area or subprogram area) has been written to a different area (for example, a subroutine SUB to RET is placed before an ED instruction). ⇒ Change to PROG. mode and enter the instruction into the correct area.	A	A	A	A	A	A	A	A

A: Available

Note) This error is also detected if you attempt to execute a rewrite containing a syntax error during RUN. In this case, nothing will be written to the CPU and operation will continue.

Error code	Name	Operation status	Description and steps to take	FP-e	FP0	FP0R	FPΣ	FP-X	FP2	FP2SH	FP10SH
E6	**Compile memory full error**	Stops	The program is too large to compile in the program memory. ⇒ Change to PROG. mode and reduce the total number of steps for the program. -FP10SH If memory expansion is possible, compilation will become possible when the memory is expanded.	A	A	A	A	A		A	A
E7	**High-level instruction type error**	Stops	In the program, high-level instructions, which execute in every scan and at the leading edge of the trigger, are programmed to be triggered by one contact. (e.g. F0 (MV) and P0 (PMV) are programmed using the same trigger continuously.) ⇒ Correct the program so that the high-level instructions executed in every scan and only at the leading edge are triggered separately.			A	A	A	A	A	A
E8	**High-level instruction operand combination error**	Stops	There is an incorrect operand in an instruction which requires a specific combination of operands (for example, the operands must all be of a certain type). ⇒ Enter the correct combination of operands.	A	A	A	A	A	A	A	A
E9	**No program error**	Stops	Program may be damaged. ⇒Try to send the program again.							A	A
E10	**Rewrite during RUN syntax error**	Continues	When inputting with the programming tool software, a deletion, addition or change of order of an instruction(ED, LBL, SUB, RET, INT, IRET, SSTP, and STPE) that cannot perform a rewrite during RUN is being attempted. Nothing is written to the CPU.						A	A	A

A: Available

11.4.2 Table of Self-Diagnostic Error

Error code	Name	Opera-tion status	Description and steps to take	FP-e	FP0	FP0R	FP Σ	FP-X	FP2	FP2SH	FP10SH
E20	**CPU error**	Stops	Probably a hardware abnormality ⇒Please contact your dealer.						A	A	A
E21	**RAM error1**	Stops	Probably an abnormality in the internal RAM. ⇒Please contact your dealer.						A	A	A
E22	**RAM error2**										
E23	**RAM error3**										
E24	**RAM error4**										
E25	**RAM error5**										
E25	**Master memory model unmatch error**	Stops	The models of master memories are different. Use the master memories created with the same model.					A *1)			
E26	**User's ROM error**	Stops	FP-e,FP0,FP0R,FP Σ ,and FP1 C14,C16:Probably a hardware abnormality. ⇒ Please contact your dealer. FP-X: When the master memory cassette is mounted, the master memory cassette may be damaged. Remove the master memory, and check whether the ERROR turns off. When the ERROR turned off, rewrite the master memory as its contents are damaged, and use it again. When the ERROR does not turn off, please contact your dealer. FP1 C24,C40,C56,C72,and FP-M: Probably an abnormality in the memory unit ⇒Program the memory unit again and try to operate. If the same error is detected, try to operate with another memory unit. FP2,FP2SH,FP10SH,and FP3: There may be a problem with the installed ROM. -ROM is not installed. -ROM contents are damaged. -Program size stored on the ROM is larger than the capacity of the ROM ⇒Check the contents of the ROM	A	A	A	A	A	A	A	A
E27	**Unit installation error**	Stops	Units installed exceed the limitations.(i.e.,4 or more link units) ⇒ Turn off the power and re-configure units referring to the hardware manual.			A	A	A	A	A	A
E28	**System register error**	Stops	Probably an abnormality in the system register. ⇒ Check the system register setting or initialize the system registers.						A		

*1) This error occurs on FP-X Ver2.0 or later.

A: Available

Error code	Name	Opera-tion status	Description and steps to take	FP-e	FP0	FP0R	FP Σ	FP-X	FP2	FP2SH	FP10SH
E29	**Configu-ration parameter error**	Stops	A parameter error was detected in the MEWNET-W2 configuration area. Set a correct parameter.						A	A	
E30	**Interrupt error 0**	Stops	Probably a hardware abnormality. ⇒ Please contact your dealer.								
E31	**Interrupt error 1**	Stops	An interrupt occurred without an interrupt request . A hardware problem or error due to noise is possible. ⇒ Turn off the power and check the noise conditions.	A	A	A	A	A	A	A	A
E32	**Interrupt error 2**	Stops	There is no interrupt program for an interrupt which occurred. ⇒ Check the number of the interrupt program and change it to agree with the interrupt request..	A	A	A	A	A	A	A	A
E33	**Multi-CPU data unmatch error**	CPU2 Stops	This error occurs when a FP3/FP10SH is used as CPU2 for a multi-CPU system. ⇒Refer to “Multi-CPU system Manual”.							A	A
E34	**I/O status error**	Stops	An abnormal unit is installed. -FP Σ, FP0R(FP0R mode),FP-X, FP2,FP2SH and FP10SH: Check the contents of special data register DT90036 and locate the abnormal unit. Then turn off the power and replace the unit with a new one. -FP3: Check the contents of special data register DT9036 and locate the abnormal unit. Then turn off the power and replace the unit with a new one.			A	A	A		A	A
E35	**MEWNET-F slave illegal unit error**	Stops	A unit, which cannot be installed on the slave station of the MEWNET-F link system, is installed on the slave station. ⇒Remove the illegal unit from the slave station.						A	A	A
E36	**MEWNET-F (remote I/O) limitation error**	Stops	The number of slots or I/O points used for MEWNET-F(remote I/O) system exceeds the limitation. ⇒Re-configure the system so that the number of slots and I/O points is within the specified range.						A	A	A
E37	**MEWNET-F I/O mapping error**	Stops	I/O overlap or I/O setting that is over the range is detected in the allocated I/O and MEWNET-F I/O map. ⇒Re-configure the I/O map correctly						A	A	A

A: Available

Error code	Name	Opera-tion status	Description and steps to take	FP-e	FP0	FP0R	FPΣ	FP-X	FP2	FP2SH	FP10SH
E38	**MEWNET-F slave I/O terminal mapping error**	Stops	I/O mapping for remote I/O terminal boards, remote I/O terminal units and I/O link is not correct. ⇒Re-configure the I/O map for slave stations according to the I/O points of the slave stations.						A	A	A
E39	**IC card read error**	Stops	When reading in the program from the IC memory card(due to automatic reading because of the dip switch setting or program switching due to F14(PGRD) instruction): - IC memory card is not installed. - There is no program file or it is damaged. - Writing is disabled. - There is an abnormality in the AUTOEXEC.SPG file. - Program size stored on the card is larger than the capacity of the CPU. ⇒Install an IC memory card that has the program properly recorded and execute the read once again.							A	A
E40	**I/O error**	Sele-ctable	Abnormal I/O unit. FPΣ, FP-X: Check the contents of special data register DT90002 and abnormal FPΣ expansion unit (application cassette for FP-X). Then check the unit. FP2 and FP2SH: Check the contents of special data registers DT90002,DT90003 and abnormal I/O unit. Then check the unit. Selection of operation status using system register21: -to continue operation, set 1 -to stop operation, set 0 Verification is possible in FPWIN GR/Pro at "I/O error" in the status display function. MEWNET-TR communication error FP3 and FP10SH: Check the contents of special data registers(FP3:DT9002,DT9003,FP10SH:DT90002,DT90003) and the erroneous master unit and abnormal I/O unit. Then check the unit. Selection of operation status using system register21: -to continue operation, set 1 -to stop operation, set 0 Verification is possible in FPWIN GR/Pro at "I/O error" in the status display function.				A	A	A	A	A

A: Available

Error code	Name	Opera-tion status	Description and steps to take	FP-e	FP0	FP0R	FP Σ	FP-X	FP2	FP2SH	FP10SH
E41	**Intelligent unit error**	Selec-table	An abnormality in an intelligent unit. FPΣ, FP-X: Check the contents of special data register “DT90006” and locate the abnormal FP intelligent unit (application cassette for FP-X). FP2,FP2SH,and FP10SH: Check the contents of special data registers DT90006,DT90007 and locate the abnormal intelligent unit. Then check the unit referring to its manual.. Selection of operation status using system register22: -to continue operation, set 1 -to stop operation, set 0 FP3: Check the contents of special data registers DT9006,DT9007 and locate the abnormal intelligent unit. Then check the unit referring to its manual.. Selection of operation status using system register22: -to continue operation, set 1 -to stop operation, set 0 Verification is possible in FPWIN GR/Pro at “I/O error” in the status display function.				A	A	A	A	A
E42	**I/O unit verify error**	Selec-table	I/O unit(Expansion unit) wiring condition has changed compared to that at time of power-up. ⇒ Check the contents of special data register (FP0: DT9010, FPΣ, FP-X: DT90010,DT90011) and locate the erroneous expansion unit. It checks whether an expansion connector is in agreement. ⇒ Check the contents of special data register (FP2,FP2SH,and FP10SH:DT90010,DT90011,FP3 DT9010,DT9011) Selection of operation status using system register23: -to continue operation, set 1 -to stop operation, set 0 Verification is possible in FPWIN GR/Pro at “I/O error” in the status display function.		A	A	A	A	A	A	A

A: Available

Error code	Name	Opera-tion status	Description and steps to take	FP-e	FP0	FP0R	FP Σ	FP-X	FP2	FP2SH	FP10SH
E43	**System watching dog timer error**	Selec-table	Scan time required for program execution exceeds the setting of the system watching dog timer. ⇒ Check the program and modify it so that the program can execute a scan within the specified time. Selection of operation status using system register24: -to continue operation, set 1 -to stop operation, set 0							A	A
E44	**Slave station connecting time error for MEWNET-F system**	Selec-table	The time required for slave station connection exceeds the setting of the system register 35. Selection of operation status using system register25: -to continue operation, set 1 -to stop operation, set 0						A	A	A
E45	**Operation error**	Selec-table	Operation became impossible when a high-level instruction was executed. Selection of operation status using system register26: -to continue operation, set K1 -to stop operation, set K0 The address of operation error can be confirmed in either special data registers DT9017 and DT9018, or DT90017 and DT90018. (It varies according to the model to be used.) DT9017, DT9018: FP-e, FP0, FP0R(FP0 mode) DT90017, DT90018: FPΣ, FP-X, FP0R(FP0R mode), FP2, FP2SH, FP10SH Verification is possible in FPWIN GR/Pro at “I/O error” in the status display function.	A	A	A	A	A	A	A	A

A: Available

Error code	Name	Operation status	Description and steps to take	FP-e	FP0	FP0R	FP Σ	FP-X	FP2	FP2SH	FP10SH
E46	**Remote I/O commu-nication error**	Selec-table	S-LINK error Occurs only in FP0-SL1 When one of the S-LINK errors (ERR1, 3 or 4) has been detected, error code E46 (remote I/O (S-LINK) communication error) is stored. Selection of operation status using system register27: -to continue operation, set K1 -to stop operation, set K0		A						
		Selec-table	MEWNET-F communication error A communication abnormally was caused by a transmission cable or during the power-down of a slave station. FP2, FP2SH, and FP10SH: Check the contents of special data registers DT90131 to DT90137 and locate the abnormal slave station and recover the communication condition. FP3: Check the contents of special data registers DT9131 to DT9137 and locate the abnormal slave station and recover the communication condition. Selection of operation status using system register27: -to continue operation, set K1 -to stop operation, set K0						A	A	A
E47	**MEW-NET-F attribute error**	Selec-table	In the unit on the slave station, an abnormality such as: -missing unit -abnormal intelligent unit was detected. FP2, FP2SH, and FP10SH: Check the contents of special data registers DT90131 to DT90137 and locate the abnormal slave station and recover the slave condition. FP3: Check the contents of special data registers DT9131 to DT9137 and locate the abnormal slave station and recover the slave condition. Selection of operation status using system register28: -to continue operation, set 1 -to stop operation, set 0						A	A	A
E49	**Expansion unit power supply sequence error**	Stops	The power supply for the expansion unit was turned on after the control unit. Turn on the power supply for the expansion unit at the same time or before the control unit is turned on.					A			
E50	**Backup battery error**	Conti-nues	The voltage of the backup battery lowered or the backup battery of control unit is not installed. ⇒ Check the installation of the backup battery and then replace battery if necessary. By setting the system register 4, you can disregard this self-diagnostic error.				A	A	A	A	A

Error code	Name	Opera-tion status	Description and steps to take	FP-e	FP0	FP0R	FP Σ	FP-X	FP2	FP2SH	FP10SH
E51	**MEWNET-F terminal station error**	Conti-nues	Terminal station setting was not properly performed. Check stations at both ends of the communication path, and set them in the terminal station using the dip switches.						A	A	A
E52	**MEWNET-F I/O update synchro-nous error**	Conti-nues	Set the INITIALIZE/TEST selecto1inmjvbgycfrde892 r to the INITIALIZE position while keeping the mode selector in the RUN position. If the same error occurs after this, please contact your dealer.						A	A	A
E53	**Multi-CPU I/O regis-tration error (CPU2 only)**	Conti-nues	Abnormality was detected when the multi-CPU system was used. Please contact your dealer.								A
E54	**IC memory card back-up battery error**	Conti-nues	The voltage of the backup battery for the IC memory card lowered. The BATT.LED does not turn on. Charge or replace the backup battery of IC memory card.(The contents of the IC memory card cannot be guaranteed.)							A	A
E55	**IC memory card back-up battery error**	Cont-inues	The voltage of the backup battery for IC memory card lowers. The BATT.LED does not turn on. Charge or replace the backup battery of IC memory card. (The contents of the IC memory card cannot be guaranteed.)							A	A
E56	**Incompati-ble IC memory card error**	Cont-inues	The IC memory card installed is not compatible. Replace the IC memory card compatible with FP2SH/FP10SH.							A	A
E57	**No unit for the configu-ration**	Conti-nues	MEWNET-W2/MCU The MEWNET-W2 link unit or MCU(Multi communication unit) is not installed in the slot specified using the configuration data. Either install a unit in the specified slot or change the parameter.						A	A	
E100 to E199	**Self-diagnostic error set by F148 (ERR)/P148 (PERR) instruction**	Stop	The error specified by the F148 (ERR)/P148(PERR) instruction is occurred. ⇒ Take steps to clear the error condition according to the specification you chose.	A	A	A	A	A	A		
E200 to E299		Conti-nues		A	A	A	A	A	A		

A :Available

11.4.3 Table of MEWTOCOL-COM Communication Error

Error code	Name	Description
!21	**NACK error**	Link system error
!22	**WACK error**	Link system error
!23	**Unit No. overlap**	Link system error
!24	**Transmission format error**	Link system error
!25	**Link unit hardware error**	Link system error
!26	**Unit No. setting error**	Link system error
!27	**No support error**	Link system error
!28	**No response error**	Link system error
!29	**Buffer closed error**	Link system error
!30	**Time-out error**	Link system error
!32	**Transmission impossible error**	Link system error
!33	**Communication stop**	Link system error
!36	**No destination error**	Link system error
!38	**Other communication error**	Link system error
!40	**BCC error**	A transfer error occurred in the received data.
!41	**Format error**	A command was received that does not fit the format.
!42	**No support error**	A command was received that is not supported.
!43	**Multiple frames procedure error**	A different command was received when processing multiple frames.
!50	**Link setting error**	A route number that does not exist was specified. Verify the route number by designating the transmission station.
!51	**Transmission time-out error**	Transmission to another device not possible because transmission buffer is congested.
!52	**Transmit disable error**	Transmission processing to another device is not possible.(Link unit runaway, etc.)
!53	**Busy error**	Command process cannot be received because of multiple frame processing. Or, cannot be received because command being processed is congested.
!60	**Parameter error**	Content of specified parameter does not exist or cannot be used.
!61	**Data error**	There was a mistake in the contact, data area, data number designation, size designation, range, or format designation.
!62	**Registration over error**	Operation was does when number of registrations was exceeded or when there was no registration.
!63	**PC mode error**	PC command that cannot be processed was executed during RUN mode.

Error code	Name	Description
!64	**External memory error**	An abnormality occurred when loading RAM to ROM/IC memory card. There may be a problem with the ROM or IC memory card. -When loading, the specified contents exceeded the capacity. -Write error occurs. -ROM or IC memory card is not installed. -ROM or IC memory card does not conform to specifications -ROM or IC memory card board is not installed.
!65	**Protect error**	A program or system register write operation was executed when the protect mode (password setting or DIP switch, etc.)or ROM operation mode was being used.
!66	**Address error**	There was an error in the code format of the address data. Also. when exceeded or insufficient of address data, there was a mistake in the range designation.
!67	**No program error and No data error**	Cannot be read because there is no program in the program area or the memory contains an error. Or, reading was attempted of data that was not registered.
!68	**Rewrite during RUN error**	When inputting with programming tool software, editing of an instruction (ED, SUB, RET, INT, IRET, SSTP, and STPE) that cannot perform a rewrite during RUN is being attempted. Nothing is written to the CPU.
!70	**SIM over error**	Program area was exceeded during a program write process.
!71	**Exclusive access control error**	A command that cannot be processed was executed at the same time as a command being processed.

11.5 MEWTOCOL-COM Communication Commands

Table of MEWTOCOL-COM commands

Command name	Code	Description
Read contact area	RC (RCS) (RCP) (RCC)	Reads the on and off status of contact. - Specifies only one point. - Specifies multiple contacts. - Specifies a range in word units.
Write contact area	WC (WCS) (WCP) (WCC)	Turns contacts on and off. - Specifies only one point. - Specifies multiple contacts. - Specifies a range in word units.
Read data area	RD	Reads the contents of a data area.
Write data area	WD	Writes data to a data area.
Read timer/counter set value area	RS	Reads the value set for a timer/counter.
Write timer/counter set value area	WS	Writes a timer/counter setting value.
Read timer/counter elapsed value area	RK	Reads the timer/counter elapsed value.
Write timer/counter elapsed value area	WK	Writes the timer/counter elapsed value.
Register or Reset contacts monitored	MC	Registers the contact to be monitored.
Register or Reset data monitored	MD	Registers the data to be monitored.
Monitoring start	MG	Monitors a registered contact or data using the code “MC or MD”.
Preset contact area (fill command)	SC	Embeds the area of a specified range in a 16-point on and off pattern.
Preset data area (fill command)	SD	Writes the same contents to the data area of a specified range.
Read system register	RR	Reads the contents of a system register.
Write system register	WR	Specifies the contents of a system register.
Read the status of PLC	RT	Reads the specifications of the programmable controller and error codes if an error occurs.
Remote control	RM	Switches the operation mode of the programmable controller.
Abort	AB	Aborts communication.

11.6 Hexadecimal/Binary/BCD

Decimal	Hexadecimal	Binary data	BCD data (Binary Coded Decimal)
0	0000	00000000 00000000	0000 0000 0000 0000
1	0001	00000000 00000001	0000 0000 0000 0001
2	0002	00000000 00000010	0000 0000 0000 0010
3	0003	00000000 00000011	0000 0000 0000 0011
4	0004	00000000 00000100	0000 0000 0000 0100
5	0005	00000000 00000101	0000 0000 0000 0101
6	0006	00000000 00000110	0000 0000 0000 0110
7	0007	00000000 00000111	0000 0000 0000 0111
8	0008	00000000 00001000	0000 0000 0000 1000
9	0009	00000000 00001001	0000 0000 0000 1001
10	000A	00000000 00001010	0000 0000 0001 0000
11	000B	00000000 00001011	0000 0000 0001 0001
12	000C	00000000 00001100	0000 0000 0001 0010
13	000D	00000000 00001101	0000 0000 0001 0011
14	000E	00000000 00001110	0000 0000 0001 0100
15	000F	00000000 00001111	0000 0000 0001 0101
16	0010	00000000 00010000	0000 0000 0001 0110
17	0011	00000000 00010001	0000 0000 0001 0111
18	0012	00000000 00010010	0000 0000 0001 1000
19	0013	00000000 00010011	0000 0000 0001 1001
20	0014	00000000 00010100	0000 0000 0010 0000
21	0015	00000000 00010101	0000 0000 0010 0001
22	0016	00000000 00010110	0000 0000 0010 0010
23	0017	00000000 00010111	0000 0000 0010 0011
24	0018	00000000 00011000	0000 0000 0010 0100
25	0019	00000000 00011001	0000 0000 0010 0101
26	001A	00000000 00011010	0000 0000 0010 0110
27	001B	00000000 00011011	0000 0000 0010 0111
28	001C	00000000 00011100	0000 0000 0010 1000
29	001D	00000000 00011101	0000 0000 0010 1001
30	001E	00000000 00011110	0000 0000 0011 0000
31	001F	00000000 00011111	0000 0000 0011 0001
.	.	.	.
.	.	.	.
.	.	.	.
63	003F	00000000 00111111	0000 0000 0110 0011
.	.	.	.
.	.	.	.
.	.	.	.
255	00FF	00000000 11111111	0000 0010 0101 0101
.	.	.	.
.	.	.	.
.	.	.	.
9999	270F	00100111 00001111	1001 1001 1001 1001

11.7 ASCII Codes

								b7								
								b6	0	0	0	0	1	1	1	1
								b5	0	0	1	1	0	0	1	1
								b4	0	1	0	1	0	1	0	1
b7	b6	b5	b4	b3	b2	b1	b0	R \ C	0	1	2	3	4	5	6	7
				0	0	0	0	0	NUL	DEL	SPACE	0	@	P	`	p
				0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
				0	0	1	0	2	STX	DC2	"	2	B	R	b	r
				0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
				0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
				0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
				0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
				0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
				1	0	0	0	8	BS	CAN	(	8	H	X	h	x
				1	0	0	1	9	HT	EM	)	9	I	Y	i	y
				1	0	1	0	A	LF	SUB	*	:	J	Z	j	z
				1	0	1	1	B	VT	ESC	+	;	K	[	k	{
				1	1	0	0	C	FF	FS	,	<	L	¥	l	|
				1	1	0	1	D	CR	GS	-	=	M	]	m	}
				1	1	1	0	E	SO	RS	.	>	N	^	n	~
				1	1	1	1	F	SI	US	/	?	O	_	o	DEL

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Record of changes

Manual No.	Date	Desceiption of changes
ARCT1F320E ACG-M320E	Jul.2000	First edition
ARCT1F320E-1 ACG-M320E-1	Jul.2003	2^{nd} edition
ARCT1F320E-2 ACG-M320E-2	May.2004	3^{rd} edition
ARCT1F320E-3 ACG-M320E-3	Feb.2005	4^{th} edition
ARCT1F320E-4 ACG-M320E-4	Sep.2006	5^{th} edition
ARCT1F320E-5 ACG-M320E-5	Mar.2007	6^{th} edition
ARCT1F320E-6 ACG-M320E-6	Apr.2008	7^{th} edition
ARCT1F320E-7 ACG-M320E-7	Oct.2008	8^{th} edition
ARCT1F320E-8 ACG-M320E-8	Feb.2009	9^{th} edition
ARCT1F320E-9 ACG-M320E-9	Mar.2009	10^{th} edition
ARCT1F320E-10 ACG-M320E-10	Jan.2010	11^{th} edition
ARCT1F320E-11 ACG-M320E-11	Apr.2011	12^{th} edition
ARCT1F320E-12 ACG-M320E-12	Sep.2012	13^{th} edition

Please contact ....

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